WLCSP Fully Protected Fan-In Reliability

Oct 2023

Doug Hackler (American Semiconductor)

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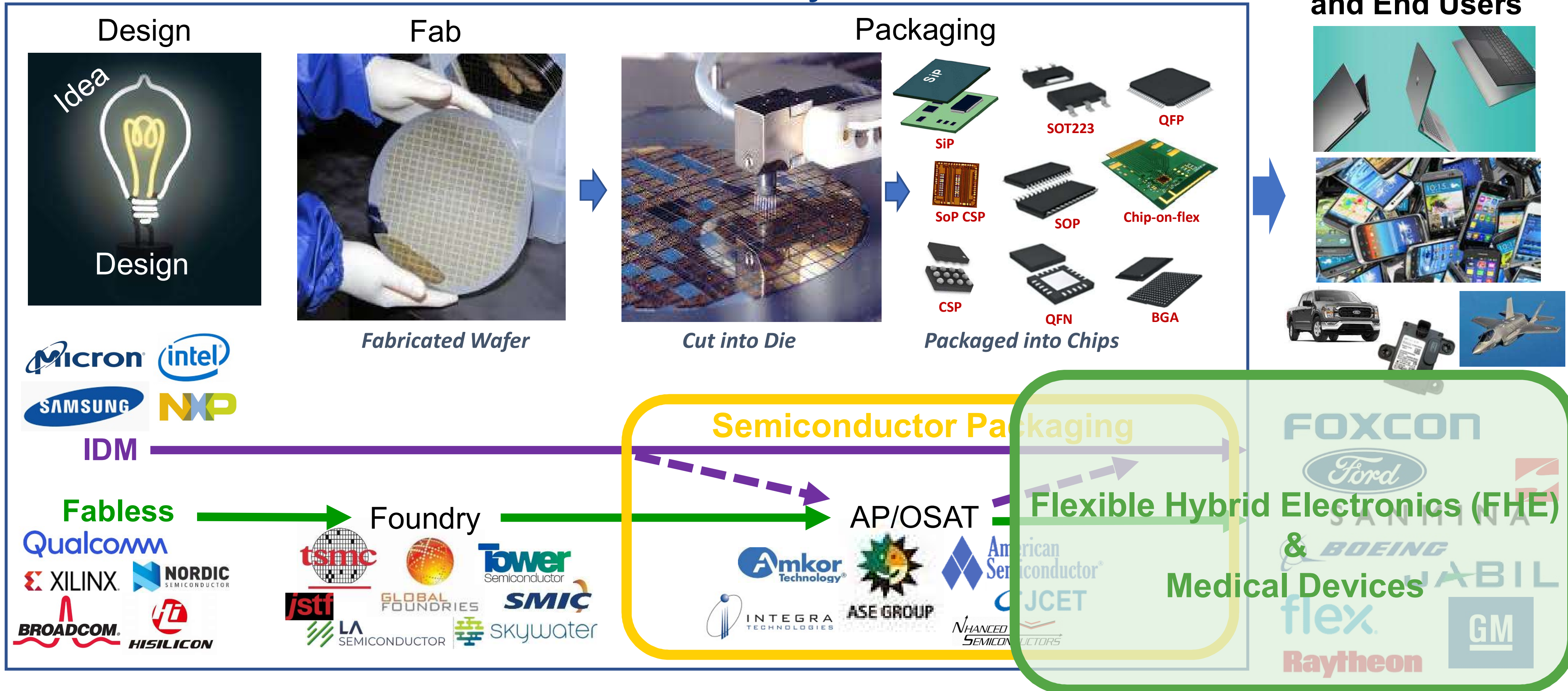
Semiconductor - Industry at a glance



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Advanced Packaging (AP) and Flexible Hybrid Electronics (FHE)

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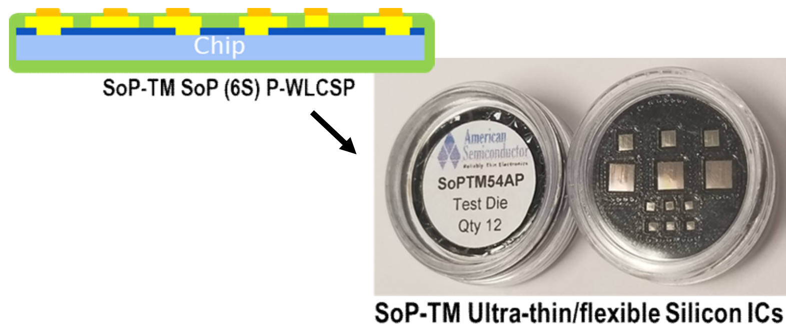
IMAPS 2023

Advanced Packaging (AP) is not defined by the things it builds; Advanced Packaging is defined by how things are built.

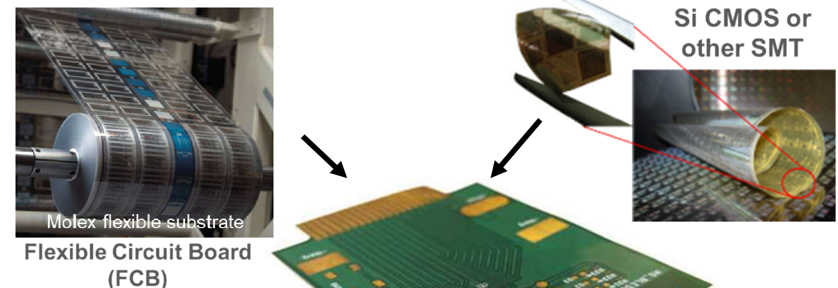
AP Packaging Technology

- Laser lithography
- Direct write and Adaptive Processing
- Ultra-thin silicon fabrication
- Thin die, flip-chip, polymer film dry release, automation,…



Flexible Hybrid Electronics (FHE)

A manufacturing technology to produce flexible hybrid systems (FHS)

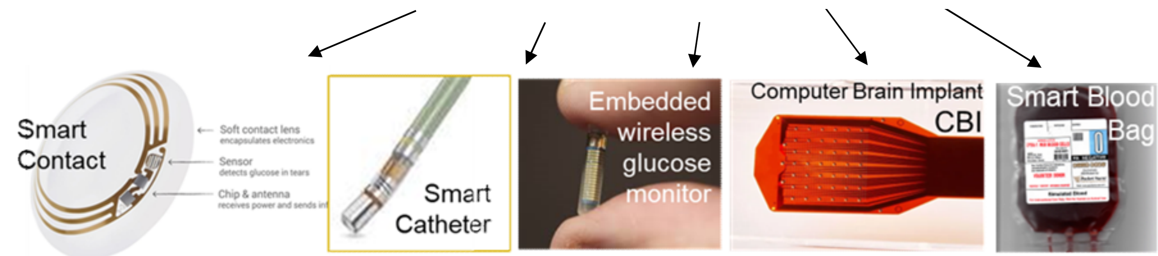


FHS

Ex: BLE Development Kit

AS_DEVBLES02.kit

Next Generation Medical Devices



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Advanced Packaging isn’t just HI

Advanced Packaging (AP) is not defined by the things it builds; Advanced Packaging is defined by how things are built.

AP must be used if on-shore manufacturing is to be feasible.

Single-chip packaging

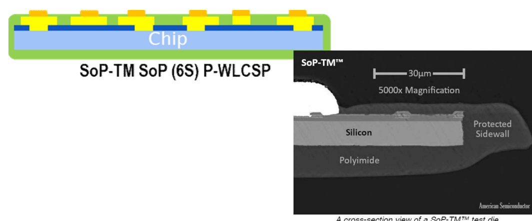
CSP, BGA, SON…

Cost is king, Reliability is required

THE CRITICAL SUPPLY CHAIN SECURITY ISSUE

Commercialization in Progress

AP: P-WLCSP



50% fewer steps
50% Less labor cost
30-50% Less material cost

Multi-chip Packaging

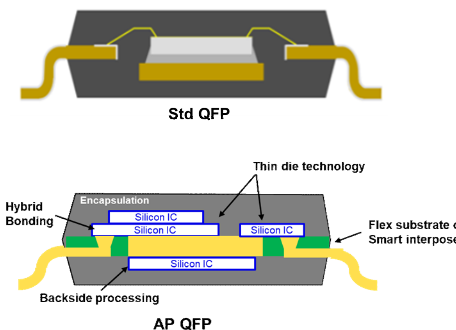
HI/SiP/MCM…

One size doesn’t fit all

Performance is king, Reliability is required

U.S. Strategic Issue

Planned Development



Specialized Packaging

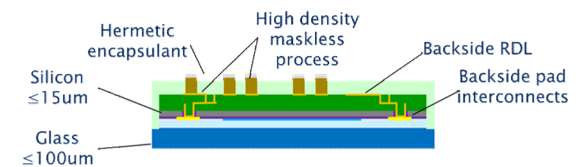
Imager/RF/Photonic…

Function & Cost, King&Queen?

Reliability is required

U.S. Strategic Issue

NSF Program Pending



AP: BSI Imager Package

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6-side protection: P-WLCSP

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- “Protected WLCSP” (P-WLCSP) resolves Cost and Complexity of non-WL for FI
  - 6-side protection without the cost and complexity on non-WL FO type processes
  - P-WLCSP does not require pre-package die thinning, dicing or reconstitution
  - P-WLCSP Substantially reduce the equipment and process steps required for processing
  - Material reductions with the elimination of dicing tape and molding materials
- Example: SoP-TM™ 6-side protected P-WLCSP introduced at IMAPS 2021
  - Full protection, without the cost/complexity of non-WL FO processes used for protected CSP FI
  - 300mm process utilizes polyimide for encasement
  - The process includes maskless processing and high temperature temporary bonding
  - Adaptive processing expands the selection of PIs available for stress balancing
  - Final singulation (dicing) speed enhancement due to P-WLCSP PI scribe streets
- Enabling ultra-thin devices
  - Reduced die thickness improves capability for through silicon via (TSV) size and pitch
  - Enables high-temperature backside RDL (B-RDL) and heat sinks
  - CMOS silicon thicknesses is typically 10-15um, but can be adjusted as needed

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SoP-TM vs non-WL CSP

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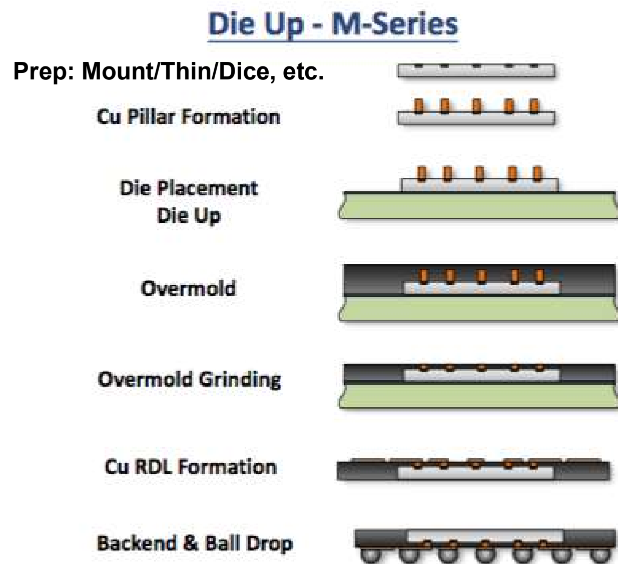
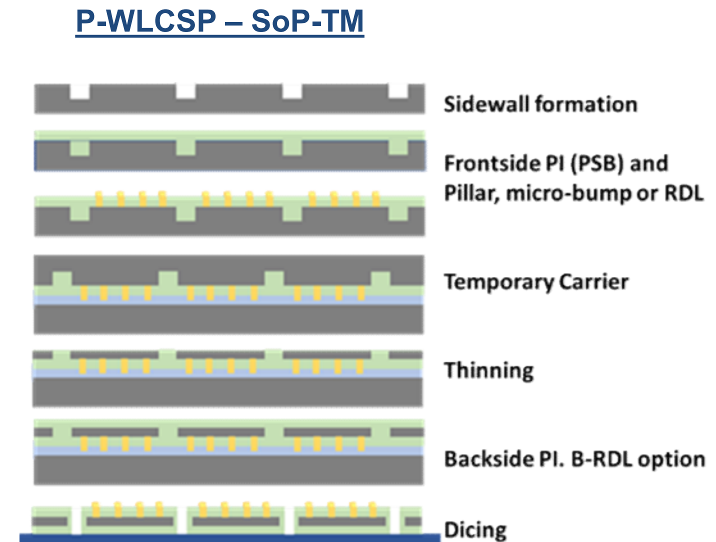
- Non-WL CSP vs P-WLCSP SoP illustrates advanced packaging benefits for FI



M-Series CSP FO Process. Source: SemicondcutorEngineering Feb. 2018



FleX-TM Protected WLCSP, U.S. Patent 9,082,881

- P-WLCSP provides cost reduction and performance improvement in CSP FI applications
- **50% fewer steps –> 50% less capital, or 2X capacity increased for existing facilities**
- **50% Less labor cost –> Cycletime 50% less, improves cash flow**
- **30-50% Less material cost**

SoP-TM – Enables On-Shore Manufacturing

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2022 Adaptive Processing

Adaptive Processing

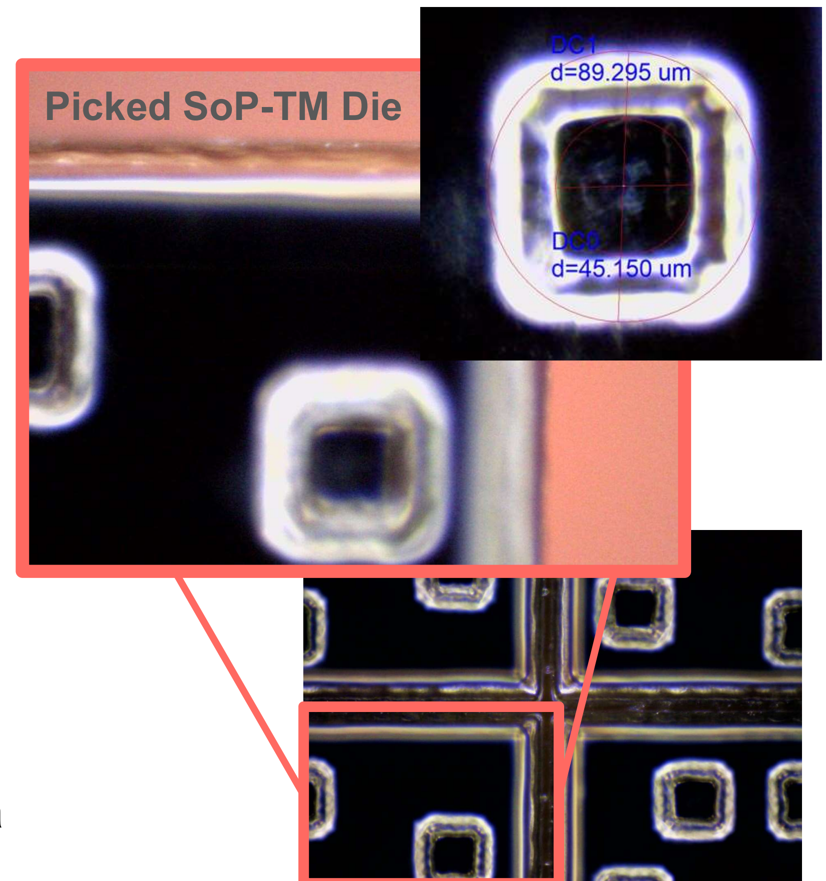
- Adaptive processing with direct write
- Maskless processing during RDL steps such as for via.

High Speed SoP Dicing

- Multi-pass recipe proves 200 mm/s effective cut speed
- Low power of 1.25 Watts.
- SoP polyimide encasement cuts cleanly without scorching
- Smooth cut line without need of protective coatings/cleans

Throughput (pre-production tool)

- Demonstrated at 4-5 WPH for 2 mm die on a 200 mm wafer.



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2023 SoP-TM process release

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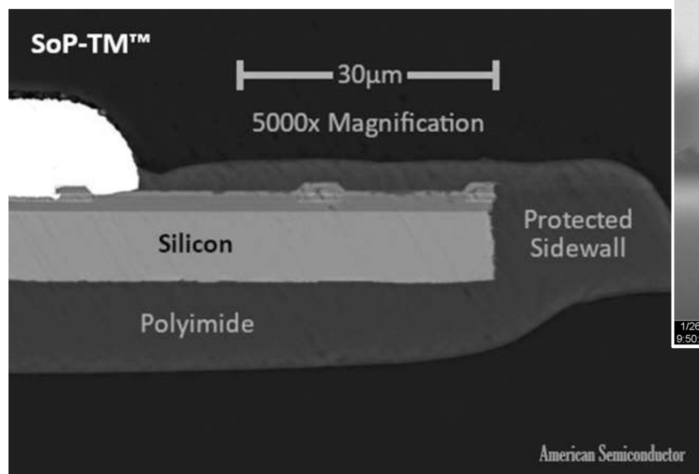
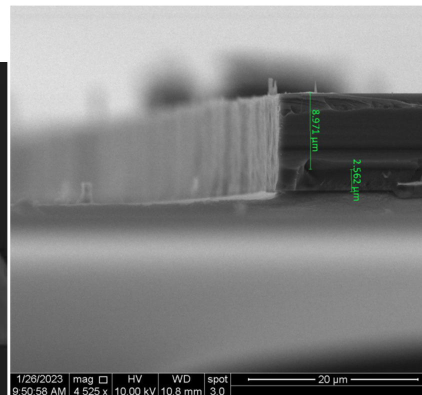
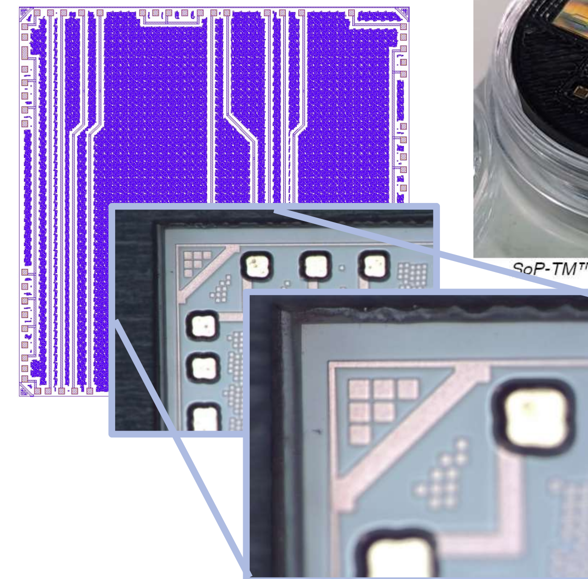
DPC2023 – Process Release and Test Chips

SoP-TM has been released for early industry adoption. The high-efficiency P-WLCSP process for protected FI includes ultra-thin package capability and is supported with Test Chips for assembly verification and development and Chip-on-flex assembly services.





A cross-section view of a SoP-TM™ test die



AS_SoPTM54AP_A.fxd Test Chip

SoP-TM™ Test Die Samples in case

Early Adopters: ***SoP-TM – Medical Device and AR/VR wearables***

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Reliability, the required foundation for AP

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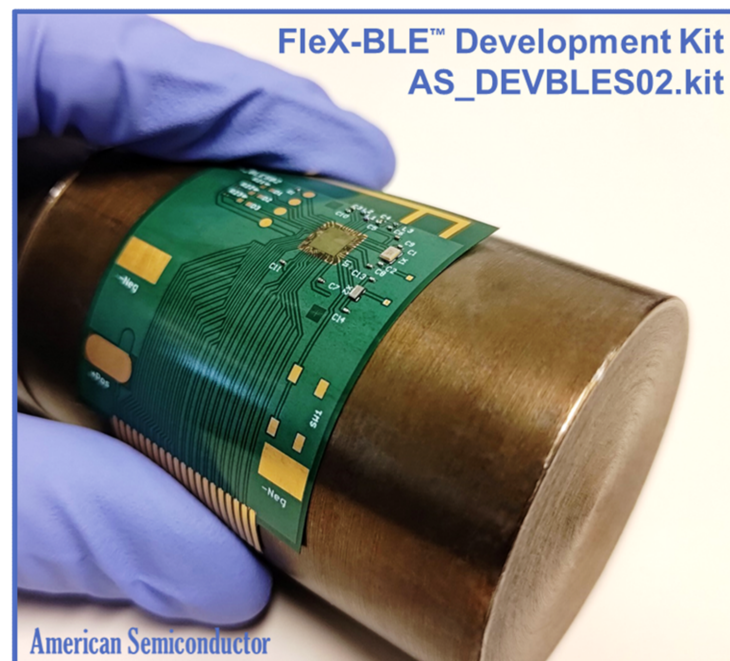
Advanced Materials, Methods, Processes and Packages often require new approaches for reliability evaluation and failure analysis

Flexible/Conformable P-WLCSP ICs on flex are being introduced for wearables, implants, sensors, labels, machine interfaces, rapid diagnostics and more.

- These novel medical devices rely on leading-edge thin and flexible microelectronics, but are they reliable?
- Bending, Twisting and Stretching are new requirements that are not typical of standard microelectronic systems.
- Development of test methods, systems and reporting of new reliability data for flexible medical electronics is needed to support this new technology



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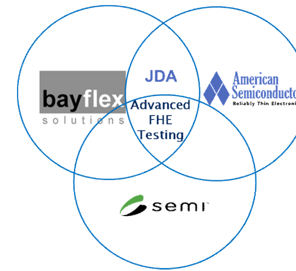
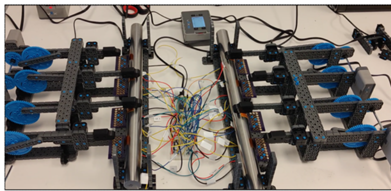
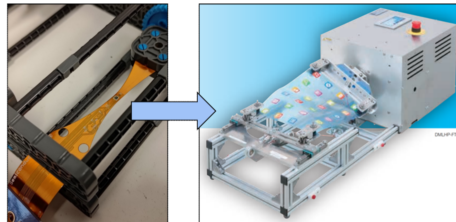
Reliability: ASI, Bayflex/Yuasa & SEMI Standards

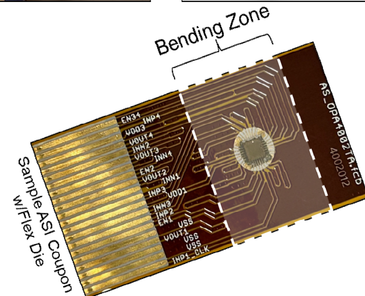


- American Semiconductor and Bayflex Solutions Joint development supporting SEMI Standards Development
  - SEMI Standards Committee Approved 9/18/2023
- Based on ASI FHE Test Development (2016 AFRL)
- TEST Equipment & Methods Development

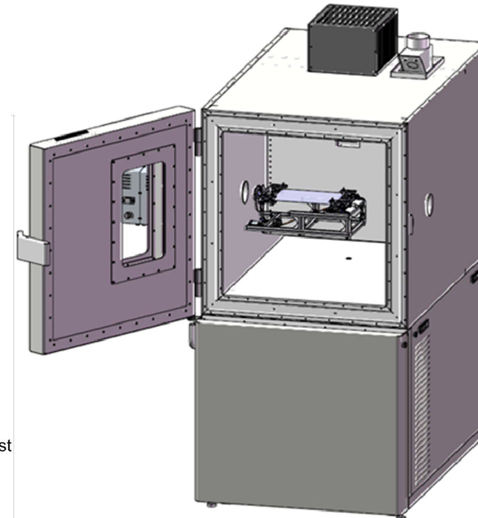
Test	Conditions	ASI Procedure	References
High Temp Life	125°C	ASI TEST008	ISO 10373-1; JESD22-A108
Low Temp Life	-25°C	ASI TEST009	JESD22-A108
ESD	HBM and/or CDM	ASI TEST010	ANSI-ESDA-JEDEC_JS-001 & JS-002
Static Radius of Curvature	Concave/Convex Bend	ASI TEST003	ASTM D522-93a; ISO 10373-1; ISO 7816
Dynamic Radius of Curvature	Concave/Convex Bend	ASI TEST005	ASTM D522-93a; ISO 10373-1; ISO 7816
Axial Torsion	Twist Test	ASI TEST006	ISO 10373-1; ISO 7816
SEM Inspection	Post SoP Conversion	ASI TEST007	MIL-STD-883: M2018
Data Retention	150°C, non-biased	ASI TEST009	JESD22-A117; JESD-A103


ASI Home Built Radius of Curvature Tester





Bayflex/ASI ROC Endurance Test



Bend
Twist
Stretch
Temperature
Humidity
Pressure
HAST,TC, THB,
LTOL, HTOL…

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Semiconductor-on-Polymer Reliability

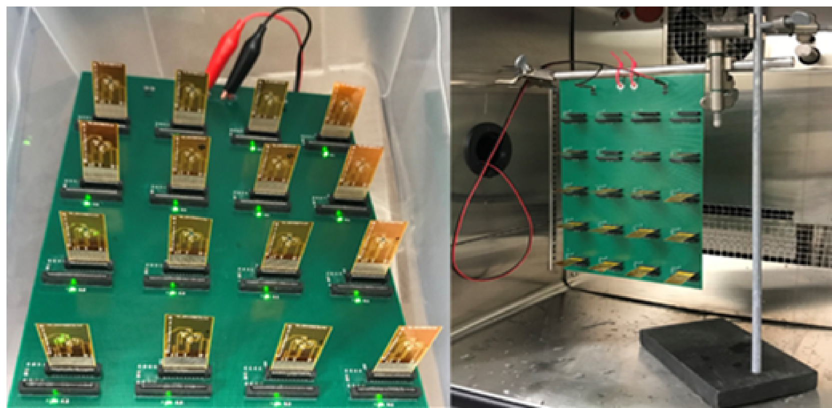
SoP-TM P-WLCSP ADA4505-1

Low Temperature Test (LTOL):
- 168 hours @ -25C, 1atm, n/a RH
- 2.5mV DC bias between VDD and VSS

Low Humidity Test (THB):
- 168 hours @ STP (22C/1atm), <10%RH
- 2.5mV DC bias between VDD and VSS

High Temperature Test (HTOL):
- 168 hours @ 125C, 1atm, n/a RH
- 2.5mV DC bias between VDD and VSS

High Humidity Test (THB):
- 168 hours @ STP (22C/1atm), 90%RH
- 2.5mV DC bias between VDD and VSS



SoP DUT on coupon on test board in environmental chamber

Data Collection: pre and post exposure, with midpoint

- Mid-point: 84 hours functional verification of 30mV p-p Gain
  - ✓ All coupons passed functionality test with 1 coupon showing increased gain.
- Final: 168 hours with full electrical characterization.
  - ✓ No test showed any consistent shift in data compared to post-assembly.
  - ✓ 2 coupons failed, failure mode indicating handling damage

Result: No significant impact from environmental exposer on electrical performance of SoP ADA4505.

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Die Strength Comparison

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Static RoC Testing (TEST003)

Manual conformance to RoC mandrel

	Process	DBG	P-WLCSP FeX-C				
	Device	Bare Die	IDM-A	IDM-B	Test Die	Fabless A	Fabless A
	Sidewall	Blade	Blade	Blade	Laser	Laser	Blade
	Dimensions	~2x2	~2.5x2.5	~3.8x3.8	~1x1	~1x1.5	~1x1.5
	Si Thickness	100 um	15 um	15 um	12 um	12 um	12 um
RoC	Bend Orientation						
20mm	Perp	P	P	P	P	P	P
	Orth	P	P	P	P	P	P
15mm	Perp	P	P	P	P	P	P
	Orth	X	P	P	P	P	P
12mm	Perp	X	P	P	P	P	P
	Orth	X	P	P	P	P	P
10mm	Perp	X	P	P	P	P	P
	Orth	X	P	P	P	P	P
8mm	Perp	X	X	P	X	X	P
	Orth	X	P	P	X	X	P
7mm	Perp	X	X	x	X	X	P
	Orth	X	P	P	X	X	P
6mm	Perp	X	X	X	X	X	P
	Orth	X	P	P	X	X	X
5mm	Perp	X	X	X	X	X	P
	Orth	X	X	X	X	X	X

	Process	DBG Thin Die					SoP-TM			SoP-TM		
	Device	Bare Silicon - Test Die					Blank Si - Test Die			AS_OPA4505P.fxd		
	Sidewall	Blade					Etch			Etch		
	Size (mm)	5					2			1.5		
	Si Thickness	100 um					12 um			10 um		
RoC	Tag ID / Bend Orientation	8A	8B	8C	8D	8E	7A	7B	7C	W3-C1	W3-C2	W3-C3
20mm	Perp	P	P	P	P	P	P	P	P			
	Orth	X	P	P	X	P	P	P	P			
15mm	Perp	X	X	P	X	X	P	P	P			
	Orth	X	X	P	X	X	P	P	P			
12mm	Perp	X	X	P	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
10mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
8mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
7mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
6mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
5mm	Perp	X	X	X	X	X	P	P	P	P	P	P
	Orth	X	X	X	X	X	P	P	P	P	P	P

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Member:

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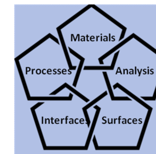
ASTN NSF Engine

Packaging, Assembly, Test and Related Services



MASIP LLC- Phoenix, AZ

MASIP LLC holistic approaches to products/markets
- Market and materials/process trends (IC pkg focus)
- Manufacturing optimization (FA and rel assessments)
- Material and process development & implementation
- Specific application materials and process assessment

Wide experience:
- Electronics-FAB, packaging and assembly
  - early publications and patents for FI & FO (RCP)
- **Material and development**
  - Implemented 1st 2 PSPSI materials at Motorola
  - IP on materials/processes for WSS/flux/AM
- **Material/interface experience and Rel modeling**
  - Solving failure mechanisms (surface/interfaces)
  - Appling material principles to key areas
    - Reliability modeling, Processing, Materials
- **Optimization of plastic package for high reliability**
    - Materials, processes, interfaces

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SoP reliability test and integration supported in part through Joint Development with Bayflex Solutions

SoP packaging supported in part through Joint Development with HD MicroSystems

Special thanks to Plasma-Therm for their support of special processing requirements

Thank You

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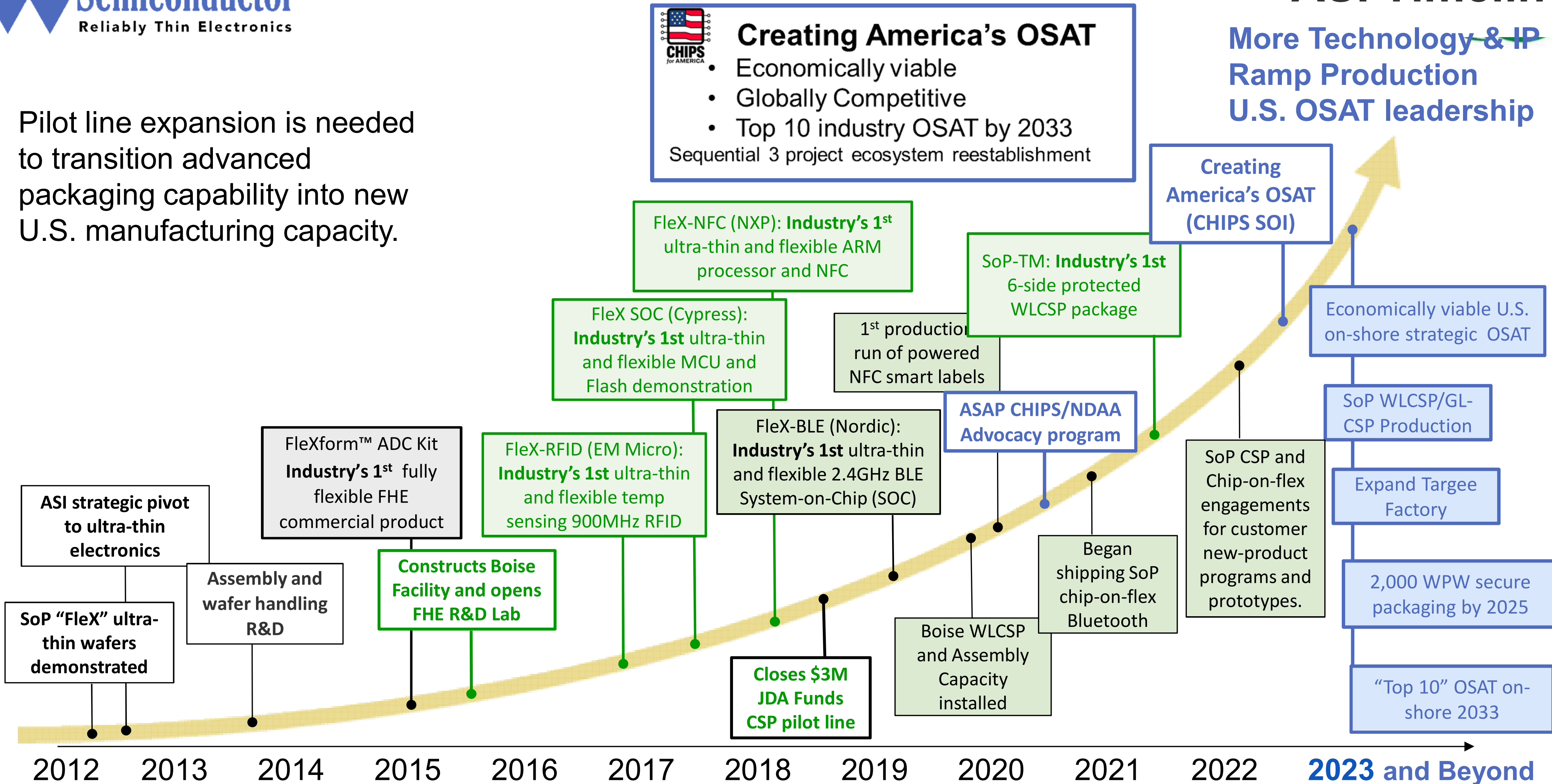

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