8th Advanced Technology Workshop on
**Advanced Packaging for Medical Microelectronics**

# Ultra-thin Flexible ICs for Smart Contacts

February 8, 2023

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American Semiconductor

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# Smart Contacts – What will it take?

## Motivation:

**Kedar Shah, Verily Life Science**

7th Advanced Tech. Workshop on Adv. Pkg for Med. Micro.

What will it take?

- Bio-compatible flex circuits
- Hermetic packaging
- Flip-chip bonding
- Wafer thinning, grinding, dicing
- 2.5 and 3D integration
- Polymer Silicon Integration
- Flexible Electronics

**The need for non-planar ICs**
- Spherical compatibility
- Available for all CMOS processes

**Hermeticity requirements**
- Pick your strategy
- Feasible polyimide integrations

**Assembly methods**
- Mounting and interconnects

**Packaging Methods**
- Ultra-thin and strong die

**Flexible Electronics**
- Testing & Verification

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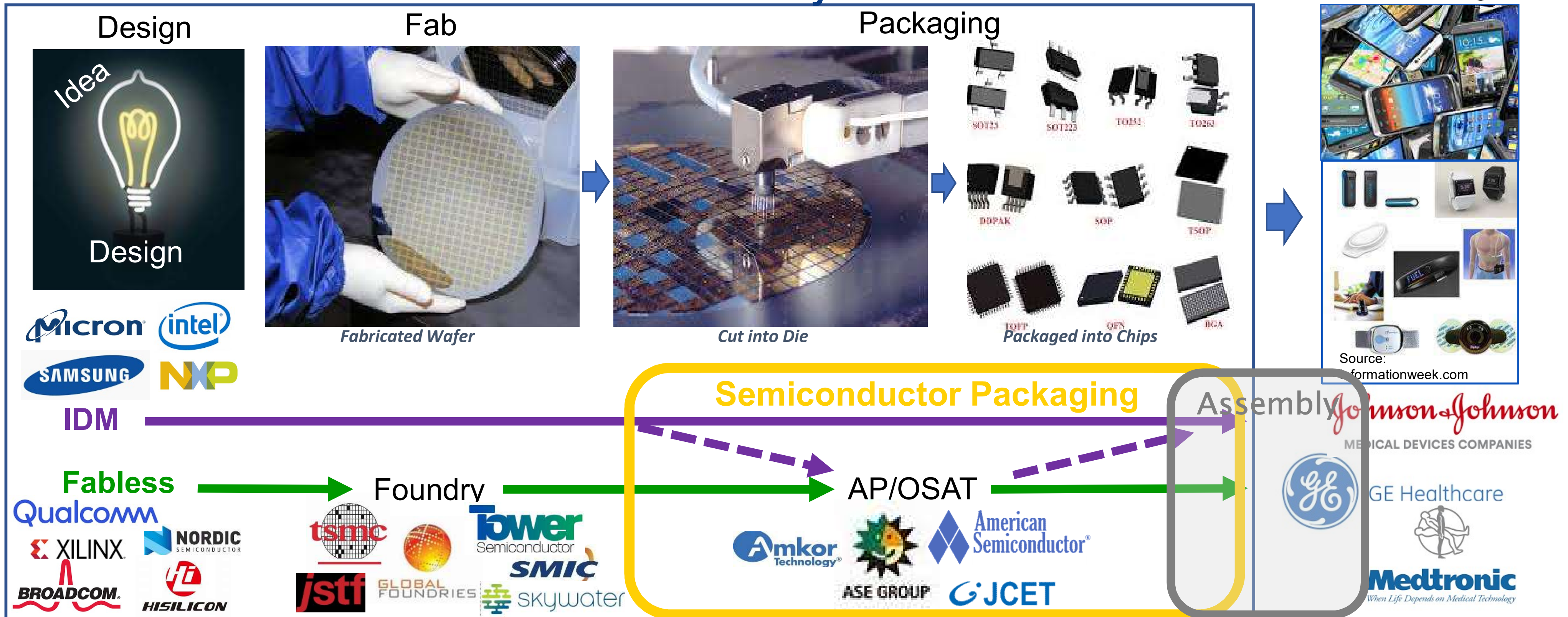
# Electronics Opportunity

Advanced Packaging and Assembly can provide product form factors needed to address the limitation and inadequacies of current microelectronics

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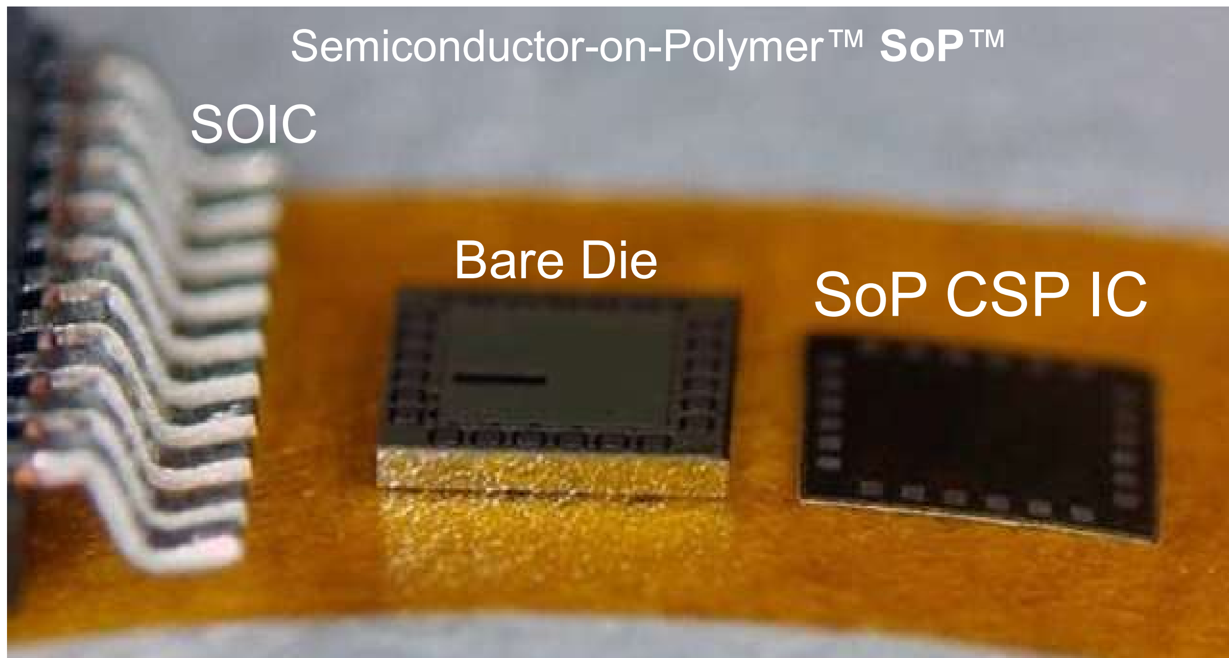
# Thin IC Packaging

iMAPS

Ultra-thin and flexible package for CMOS ICs




SoP P-WLCSP technology makes the ***thinnest chips possible,***
***and, they are flexible.***

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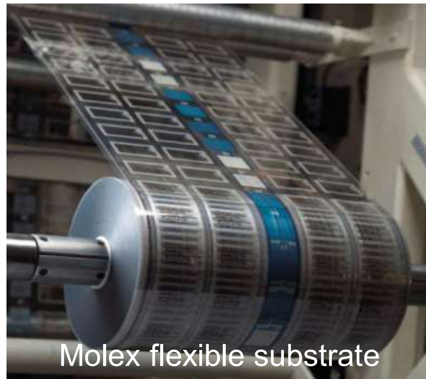
# Chip-on-flex Assembly

## Flexible Hybrid System

"Combining thin FCB and flexible silicon-based ICs creates a new class of flexible electronics."

### Flex or Printed Flexible Circuit Board (FCB)

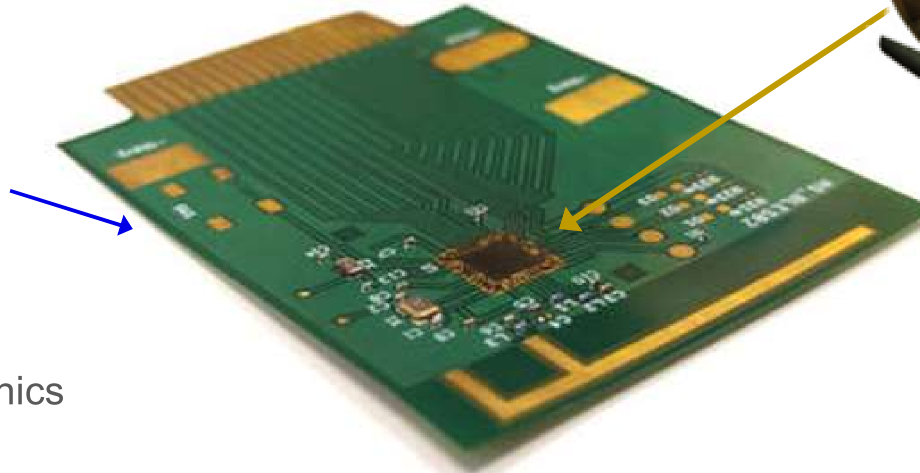
**R2R, S2S, Large Format**




Flex and Printed Electronics

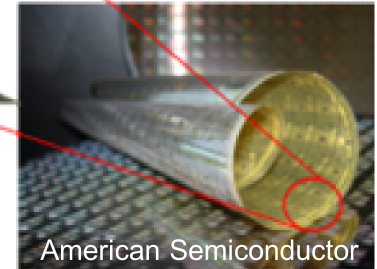
- Sensors
- Interconnects
- Antennas
- Displays

- Low Cost, Large Format
- Roll-To-Roll, Screen, Inkjet Print, …



### Ultra-thin SoP packaged ***FleX***-ICs

**High Performance, High Density**




***FleX***-ICs

- Bluetooth® SOC
- Data Processing
- Data Storage
- Communications
- Low Cost, High Performance
- ***FleX*** is a Semiconductor-on-Polymer (SoP) **chip scale packaging (CSP)** process.

Ultra-thin

**FleX-BLE Development Kit AS_DEVBLES02.kit**

***FHE enabling thinnerization***

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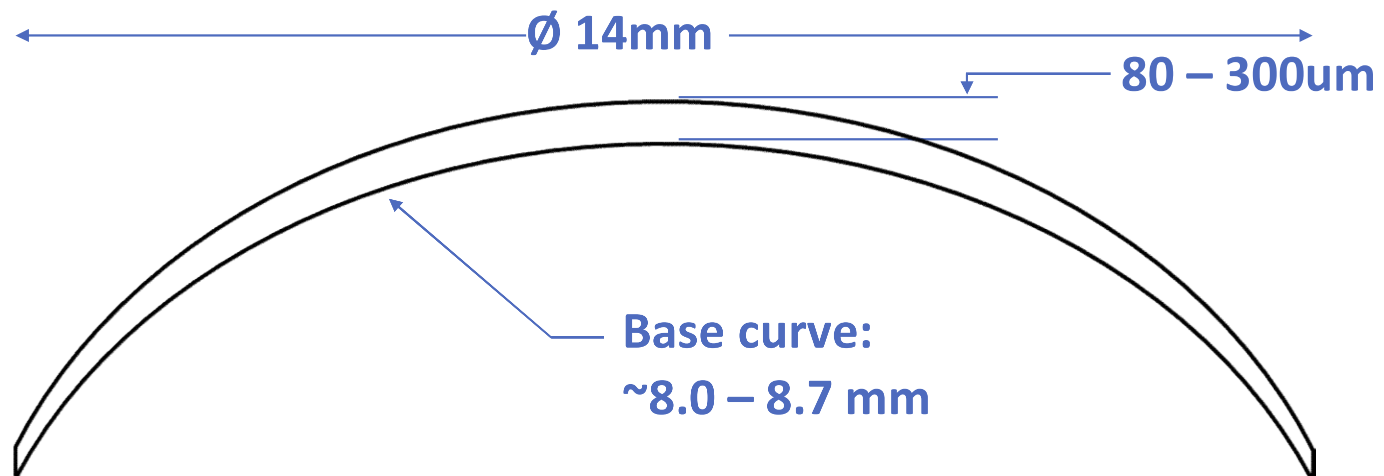
# Contact Lens Form-factor

Chips for Smart Contacts Must:

- Fit in the lens
- Be compatible
- Bend




Source: Verily Life Science 2022

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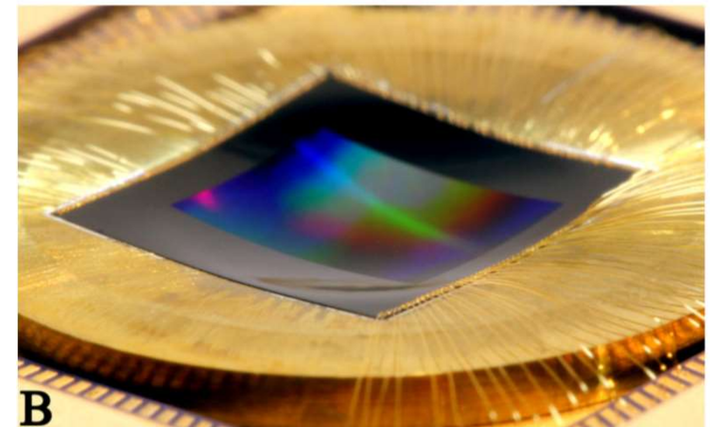
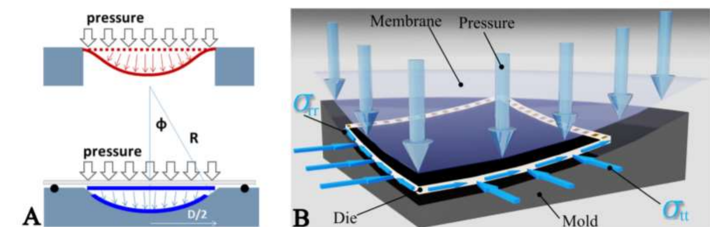
# Optical and Sensor Applications

**In 2017, Guenter, Joshi, et al, demonstrated benefits for "mass-producible", curved image sensors**

- Guenter achieved 24.6 - **16.7** mm RoC
- 7.6x7.7mm CMOS die
- 25um die thickness




**Pressure/Vacuum strain inducing process –** ***Microsoft/HRL 2017***
**Source:** "Highly curved image sensors: a practical approach for improved optical performance". OPTICS Express, Jun 2017

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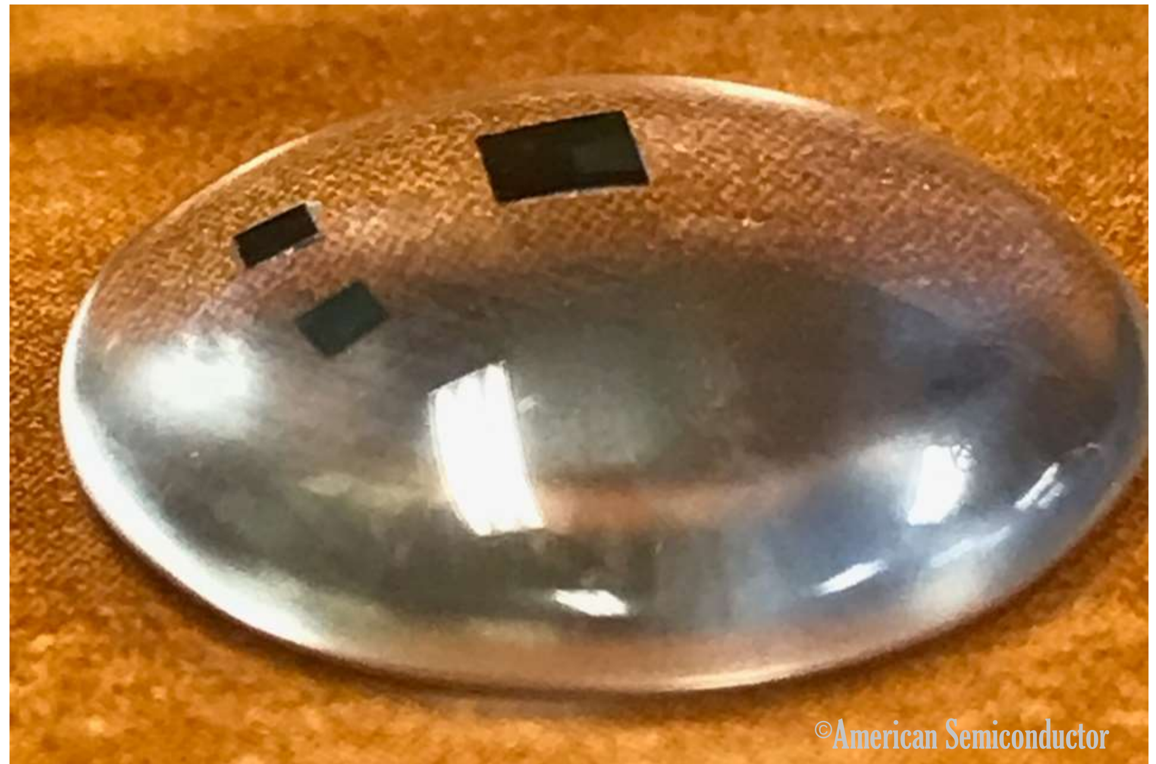
# Innovation - SoP polymerized IC packaging capability that enables hemispherical die assembly

## New IC Capability for Ocular Applications

- Hemispherical IC applications
- Package capability applicable to any semiconductor IC
- Polymerization on all 6-sides
- 2 axis bend capability
- Die radius of curvature (RoC) demonstrated to <5mm
- Hemispherical RoC demonstrated for ocular applications at <9mm

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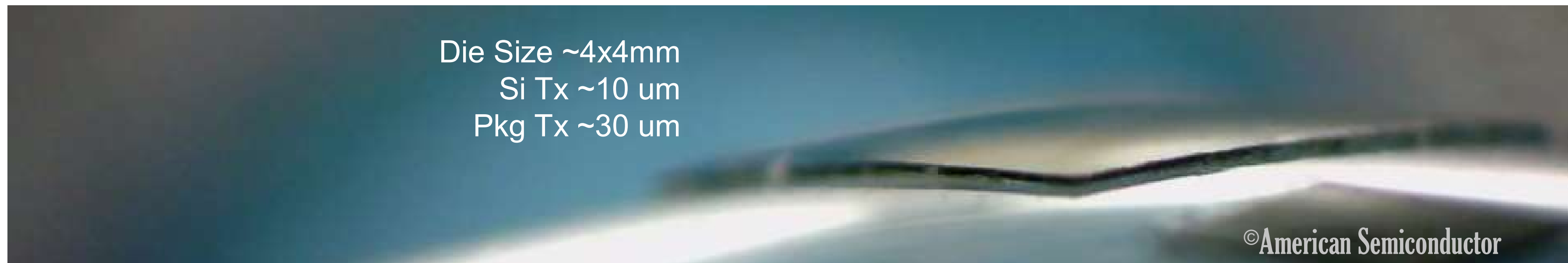
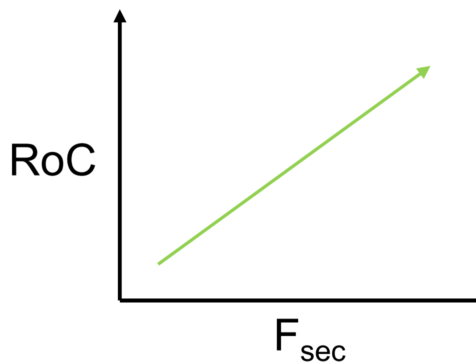
# Conformal Die Mounting
## TCMM54 SoP Flex Die



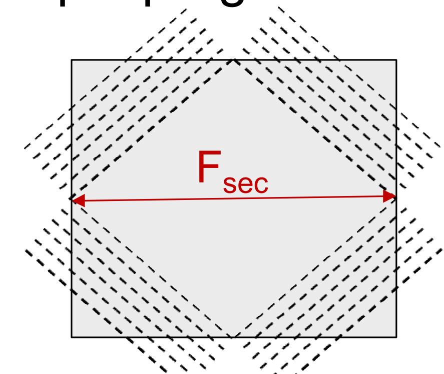

Initial R&D has confirmed single chip 2-axis bending with fold-free hemispherical assembly for SoP packaged devices. Technology fundamentals are being characterized. Prototype and demonstrator projects can make rapid progress.




**Fundamental Relationships**

- $F_{sec}$ scales with CSP area
- $CSP_{RoC}$ decreases as Tx decreases
- RoC increases as $F_{sec}$ increases

**Basic capability and reliability development is in progress**




Bend Axis for Hemi Mounting

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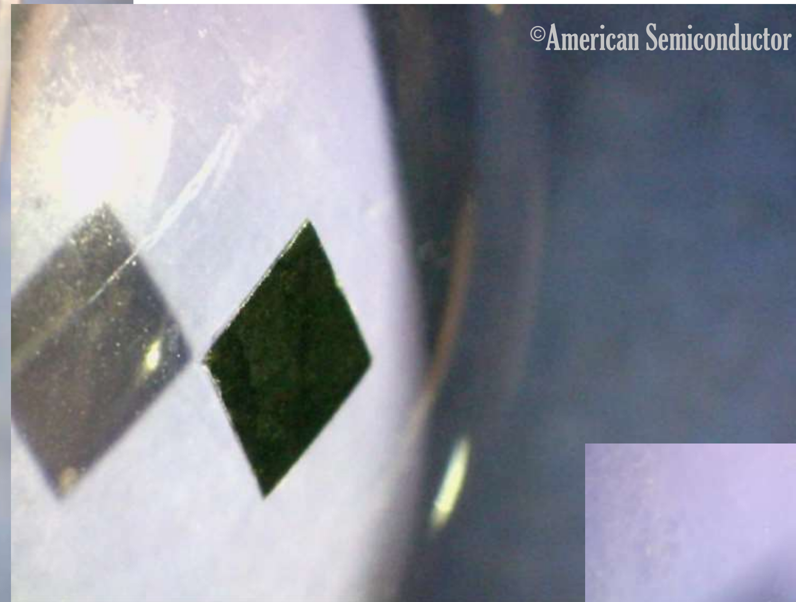
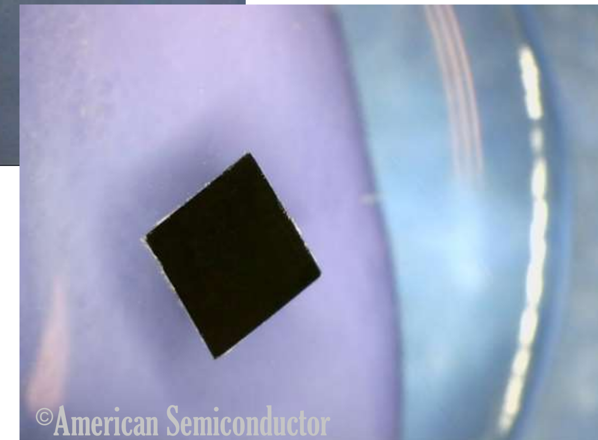
# 16mm RoC, LENS∅25mm
## 4x4mm Die Pad Down

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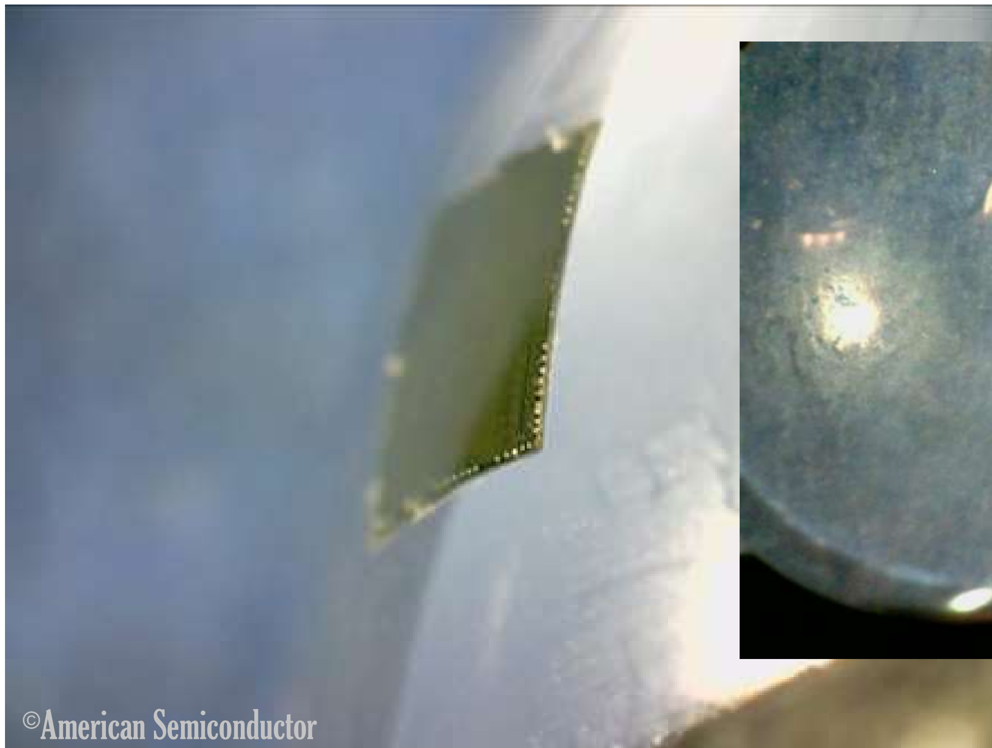
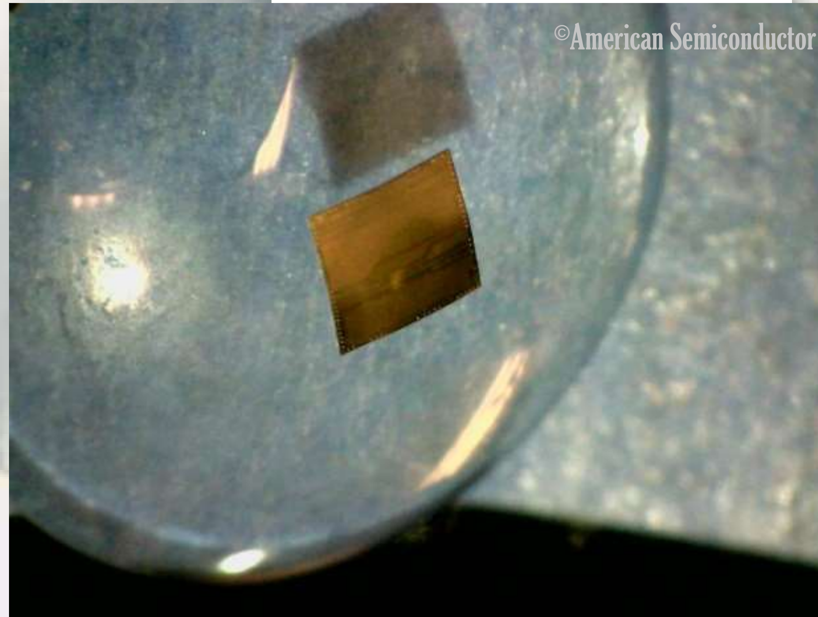
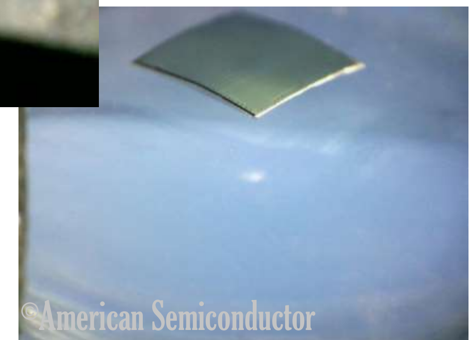
# 11mm RoC, LENS∅20mm

## 4x4mm Die Pad Up



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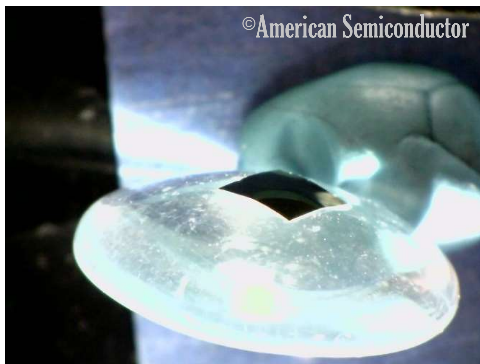
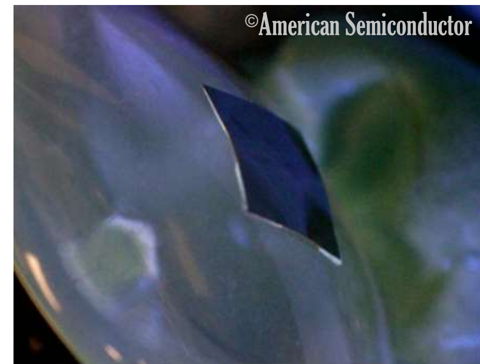
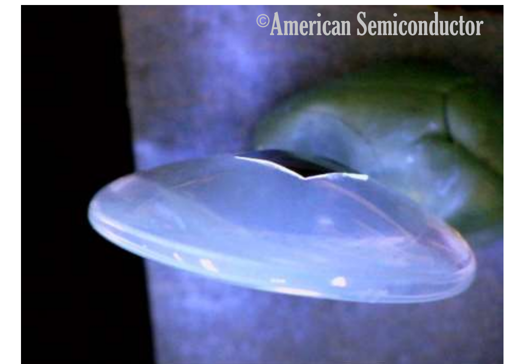
# 9mm RoC, LENS∅15mm
## 4x4mm Die Pad Down





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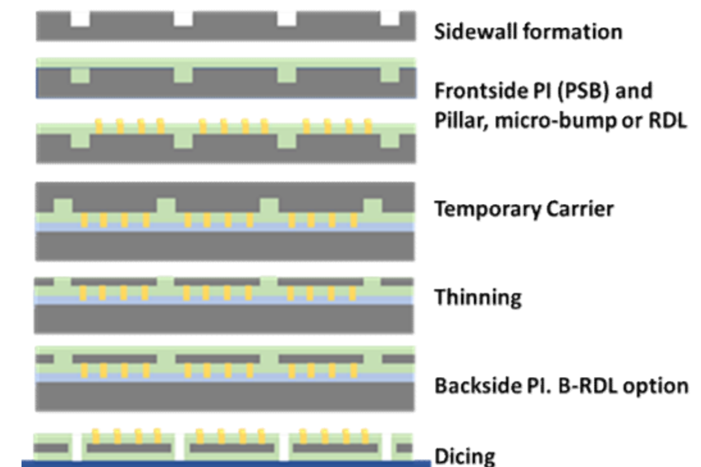
# SoP-TM™ Ultra-thin, flexible, 6-side protected, CSP

## SoP packaged ICs for hemispherical assembly

SoP-TM (6S) P-WLCSP

- True wafer level CSP process eliminates pre-packaging wafer prep:
  - No pre-package wafer grind
  - No pre-package singulation
  - No pre-package dicing tape
  - No reconstitution
- Maskless PSG
- Only 1 thinning step – utilizes clean dry release temporary adhesive
- Low cost reusable silicon carrier wafer
- Only 1 singulation step required
- Only 1 tape layer
- Standard wafer level processing for bumps, pillars and/or RDL
- Overmold process eliminated




*SoP-TM Protected WLCSP, U.S. Patent 9,082,881*

**Ultra-thin: Hemi demonstrated at 10um Si Tx**

**Available as thin as 0.2um Si Tx**

**Au Micro-bump compatible with ACA flip-chip**

***SoP – Lowest Cost Protected Fan-In***

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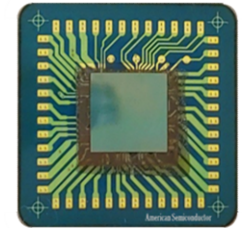
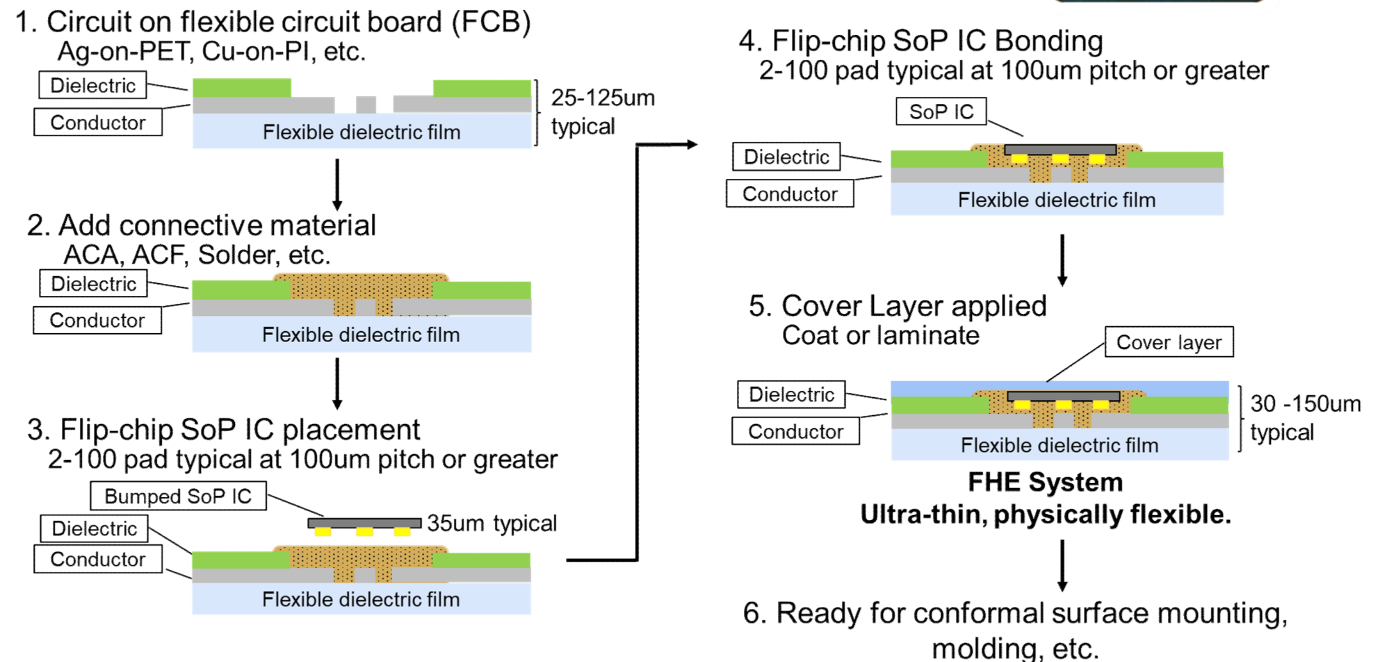
# Assembly: FleX-on-flex™ Direct Interconnect

## SoP FleX die assembly

- Direct Interconnect is used to simultaneously complete die attach and die interconnect
- ACA eliminates the need for underfill
- Flex-on-flex assemblies can run through standard lamination to add overcoats
- ACA flip-chip is compatible with standard SMT processing
- ASI maintains in-house assembly capability for ACA flip-chip manufacturing



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# Applications for chip-on-flex

- Ultra-thin chips, flexible and flexible substrates/boards
- Embed it – curve it, roll-it
- Injectable, implantable, wearable
- Reliability - Laminate encapsulants

**SoP chip-on-flex users are exploring:**
**Ocular, Brain Implant, Implanted Bluetooth™, Diagnostic insoles, Glucose Monitoring and Pharmaceutical applications**

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# American Semiconductor - Boise, Idaho

**American Semiconductor is the industry leader in ultra-thin advanced packaging. We develop state-of-the-art ultra-thin electronics technology.**

- Founded Nov. 2001
- Over 21 SBIR wins
- 2-time Boeing SOTY

**Member:**

***Packaging, Assembly, Test and Related Services***

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# ASI Seeking Partners and Collaborators

- American Semiconductor operates as an OSAT and can package ICs from any IDM or Foundry in Semiconductor-on-Polymer™ (SoP) technology
- American Semiconductor invented SoP technology and has multiple patents for SoP packaging
- American Semiconductor can provide immediate manufacturing capacity to produce SoP ICs for new programs
- Collaborator and Partner engagements may include:
  - Contracts for packaging, assembly and test services
  - Prototype or new product demonstration joint development
  - Licensing (market or application exclusivity may be considered)
  - Equity (ASI is a small business and seeks early investment in advance of CHIPS participation)
  - Other relationships as may be mutually beneficial

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# Thank You

**SoP packaging supported in part through Joint Development with HD MicroSystems**

**Thanks to Disco for their on-going support of ultra-thin processing requirements**

**Special thanks to Plasma-Therm for their support of special processing requirements**

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iMAPS

Vision correction is one of our most common and significant medical challenges. Contacts, implants and vision correction today are limited to conventional static lens technology. New applications of active device technology and materials provide the opportunity to create dynamic vision correction devices. Microelectronics miniaturization, assembly, and packaging technologies open the door to embedding electronic systems into ophthalmic devices and enable new applications that are not possible with passive ocular devices. New dynamic lens technology requires ICs that can be embedded in or on the lens, conform to the hemispherical form and control the lens shape. Ultra-thin Semiconductor-on-Polymer™ advance packaging has the ability to achieve the thickness limits that are necessary and conform to hemispherical shapes. Advanced IC packaging that enables flexible ultra-thin hemispherical shapes for conventional silicon-based devices will be presented.


- [1] K. G. Shah, SmartLenses: Needs, Opportunities, and Challenges, IMAPS 7th Advanced Technology Workshop on Advanced Packaging for Medical Technologies, 2022
- [2] D. R. Hackler Sr., E. R. Prack, Protected Wafer Level Chip Scale Packaging (P-WLCSP), IMAPS 55th International Symposium on Microelectronics, 2022.


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