Protected Wafer Level Chip Scale Packaging (P-WLCSP)

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Abstract

With the advent of bumped die, new IC packages evolved: for low IO WLCSP (wafer level chip scale package), for high IO FC (flip chip), CBGA (ceramic ball grid array), and PBGA (plastic ball grid array). For low IO, protected CSP is an emerging and rapidly growing market. In 2020 the market exceeded $2B and is ramping to a forecast $2.5B by 2025.[1] Initially WLCSP, also known as FI (fan in), was built on the wafer with no active side protection, evolving to single sided protection from a package built on the wafer[3], which transitioned to redistribution PSB (passivation stress buffer)[4]. PSBs were implemented in FC wafers for high IO BGA packages. These provided acceptable performance initially, however as devices became more complex and reliability requirements increased, these processes no longer provided the required reliability. To attain higher IO capability and better reliability, performance evolved to CSP[5] (non-WL) which allowed larger area for bump distribution and additional protection to the rest of the exposed die surfaces. An example of fully protected die CSP (without substrates or leadframes) encapsulated in mold compound is M-series utilizing a FO (fan out) processes and eWLB.[6,7] To obtain higher reliability 6-sided die protection afforded by FO processes require die reconstitution, expensive tapes, molding, and other operations which can feasibly be eliminated in a WLCSP protected FI process assuming full encapsulation can be attained on the original device wafer. American Semiconductor's Semiconductor-on-Polymer (SoP) 300mm SoP-TM, a P-WLCSP process, is an advanced packaging process optimized for protected fan-in. SoP-TM produces the thinnest and lowest cost fully protected FI. Protected FI process innovations can improve performance in power devices, RF switches, die stacking and thin board applications. This paper includes background on the evolution of CSP, comparison of SOTA (state of the art) FI processes including SoP-TM and builds on low-cost wafer level adaptive process works and reliability data presented on the new SoP-TM process earlier this year.[8,9] First article electrical reliability test data for P-WLCSP, adaptive processing of micro-bump pads, and potential applications in hybrid modules will be shown.

Key words

CSP, Fan-In, Flexible, Protected, P-WLCSP, Semiconductor-on-Polymer, SoP, Thin

I. Introduction

Wafer level packaging (WLP) is a technique for connecting packaging elements to an integrated circuit before dicing it from the wafer. Unlike the traditional approach, which involves dicing the wafer into individual die before attaching the packaging elements, WLP does not. WLP began with the advent of bumped die, and then started its evolution. WLP not includes low IO WLCSP (wafer level chip scale package), high IO FC (flip chip), CBGA (ceramic ball grid array), PBGA (plastic ball grid array) and an increasing array of WLP processes to meet market requirements for lighter, smaller, thinner, more cost-effective and especially more-reliable wafer packaging solutions.

Factors such as increased usage of high-speed, compact-size, and less expensive electronic goods are expected to propel the worldwide wafer level packaging business forward. Protected CSP, aka P-CSP with 6 side encasement for improved reliability, is an emerging and rapidly growing market. In 2020 the CSP market exceeded $2B and is ramping to a forecast $2.5B by 2025.[1] The Global WLP market is expected to reach $14.1 billion by 2028 [2], rising at a market growth of 17.7% CAGR. When first introduced, WLCSP (aka fan in or FI), was built in WLP with no active side protection, evolving to single sided protection from packages built on the wafer.[3] This transitioned to

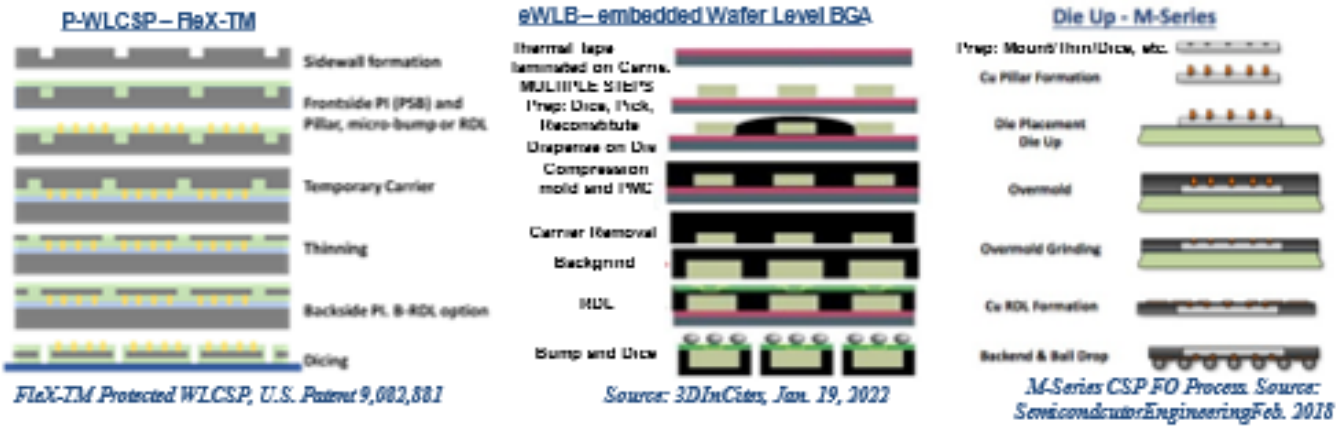
redistribution PSB (passivation stress buffer)[4]. PSBs were implemented in FC wafers for high IO BGA packages. These provided acceptable performance initially, however as devices became more complex and reliability requirements increased, these processes no longer provided the required reliability. To attain higher IO capability and better reliability, performance evolved to CSP[5] (non-WL) which allowed larger area for bump distribution and additional protection to the rest of the exposed die surfaces. Early examples of fully protected die CSP (without substrates or leadframes) encapsulated in mold compound are M-series utilizing a FO (fan out) processes and eWLB.[6,7] To obtain higher reliability 6-sided die protection afforded by FO processes require die reconstitution, expensive tapes, molding, and other operations which can feasibly be eliminated in a WLCSP protected FI process assuming full encapsulation can be attained on the original device wafer. American Semiconductor's Semiconductor-on-Polymer (SoP) 300mm SoP-TM process was first introduced at IMAPS in 2021.[8,9]

II. P-WLCSP Processes

SoP-TM is the newest P-WLCSP (protected-wafer-level-chip-scale-package) process and the first process optimized for 6s protection (encasement on all 6 die sides) without the use of reconstitution steps.

Figure 1 - SoP-TM SoP 6S P-WLCSP

The process eliminates pre-packaging wafer prep steps which eliminate tape, grinding, dicing, and reconstitution to reduce process cost and complexity. The process includes maskless PSB using adaptive processing and maskless RDL steps. Standard wafer level processing for bumps, pillars and/or RDL can be used. Only 1 thinning step is required and is implemented with a unique dry release temporary adhesive that eliminates chemical process for debonding. A low-cost recyclable silicon carrier wafer is used. Overmold processing is eliminated with application of polyimide on all 6 sided. Only 1 singulation step is required and implemented with a high-speed laser method. The process has only 1 tape step and the tape-on-frame can be used in lieu of alternatives in presentation for pick and place assembly.



- SoP processing provides cost reduction and performance improvement in P-WLCSP FI applications
- Produce robust ultra-thin devices for SiP applications - chiplets and heterogeneous integration
- Higher pin-counts and thinner board assemblies are macrotrends in modern electronics
- Reducing layer thicknesses, along with the opportunity to connect on top and bottom of die without any significant cost penalty is significant.

Fig. 2 - P-WLCSP Process Comparison

A. Adaptive Processing

Unlike adaptive patterning that adjusts laser exposers to accommodate inaccuracies of reconstituted die, adaptive processing implements direct right capability for maskless processing during RDL steps such as are common for UBM.

B. High Speed SoP Dicing

Laser dicing has been demonstrated as part of the new SoP-TM process. Current development using a multi-pass recipe resulted in a 200 mm/s effective cut speed with a low power of 1.25 Watts. At this speed and power level, SoP's polyimide encasement cuts cleanly without the typical scorched edges seen when laser cutting Si. The resulting cut line is smooth and clean without the need of a protective coating for managing laser cutting residue and debris. Throughput using a pre-production tool is demonstrated at 4-5 WPH for 2 mm die on a 200 mm wafer.

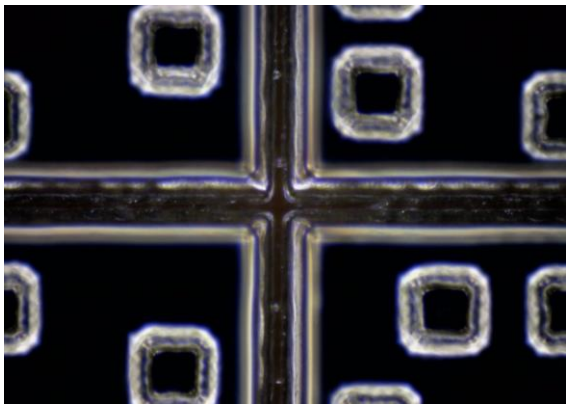


Fig. 3 - SoP-TM wafer after highspeed laser dicing

III. SoP Package Reliability

SoP-TM can be used for today's industry standard 100 um thick devices, but scales to package thicknesses well below 25 um. Current device characterization and reliability testing is being done with the ASI OPA4002 OPAMP with a silicon thickness of ~15um and a total package thickness of ~35 um.

Silicon becomes very flexible at these thicknesses. The bendable nature of the CSP devices has resulted in ASI development of test methods that add physical deformation, i.e. bending, to be included in reliability test procedures. These test procedures provide a good comparison of mechanical durability vs thicker devices as well as electrical performance during application of external device stress.

Static RoC Testing (ASI TEST003) involves SoP CSP device test results. In this mechanical test, SoP-TM test chips are forced to conform to precision mandrels at various diameters in concave and convex orientation. In this test, FleX-TM packaged die were demonstrated to pass testing from 12mm RoC (Radius of Curvature) to as little as 2.0 mm RoC. Failures for die cracking did not occur until 1.5 mm RoC.

Dynamic Bend Test (ASI TEST005) is utilized to determine durability for continued cycling of chip bending. ASI TEST005 was derived from ASTM D522-93a and utilizes test coupons with chips mounted on flex. Robotic cycling is done at specific (RoC) for bend and release in concave and convex orientation. FleX-TM test chips pass initial mechanical testing at 10 mm RoC at 10,000 cycles.

AS_OPA4002 OPAMPS ACA flip-chip mounted on Cu-on-PI test coupons were used for verification of ultra-thin silicon performance in SoP. ASI TEST005 dynamic bend testing was run at 10mm ROC for 10k cycles in each bend direction (concave/convex) for 20k total cycles. During this test, Vdd and Gain were monitored in-situ during the bend cycling using the test circuit and set-up shown in Fig. 4 and 5.

Coupon Vdd was extremely stable between 2.0V and 2.2V regardless of flexures. However, a Vdd variance down to 1.83V was observed during the test and tracked to a bad test board connection. Vdd variance due to the set-up was observed in the Gain results. Gain for the test coupons averaged 3.06dB with a range from 2.57dB to 3.49dB with a Standard Deviation of 0.0528dB. Most significantly, test coupon performance before bend testing and after bend testing remained constant.

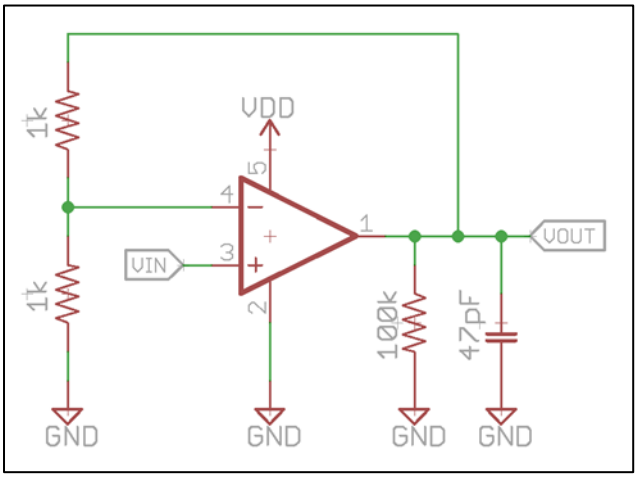


Fig. 4 - OPA4002 OPAMP circuit used for reliability tests

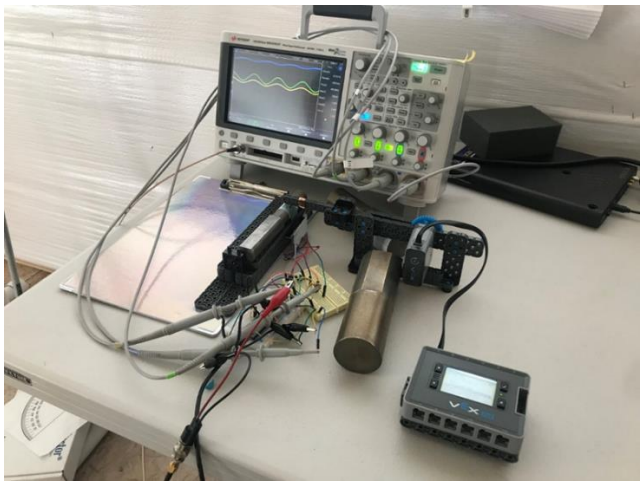


Figure 5 - OPA4002 OPAMP Set-up for reliability tests

Dynamic SoP CSP OPAMP testing motivated questioning whether or not device function changed during a bend cycle. To answer this question, AS_OPA4002 test coupons were measured under no-bend, half-bend, full-bend, half-release and full-release (no-bend) conditions. Vdd difference between no bend and full bend was only 0.013V and the Gain difference between no bend and full bend was only 0.016dB.

A. Temperature-humidity-bias (THB) Testing

In addition to RoC testing, the SoP packaging was evaluated through THB testing. Initial results are reported for THB feasibility demonstration. Full THB testing is in-progress. For the feasibility evaluation, BLE connectivity FO interposers with NRF51822P SoP CSP ACA flip-chip mounted were used for test coupons. See Fig.6.

The flip-chip connections are approximated 50um pad/50um space, 100um pitch. Electrical performance was validated with a 44 pin diode test on each sample (0.2-0.8V passing range). Electrical testing was done pre-, mid-points (each Temp Cycle), and post on every pin/sample. Low-temp Testing utilized 2 samples with Troom pre-test, -24C/72hr soak, and Troom/72hr test. Low Temp Results at -24C demonstrated 100% post-temp yield.

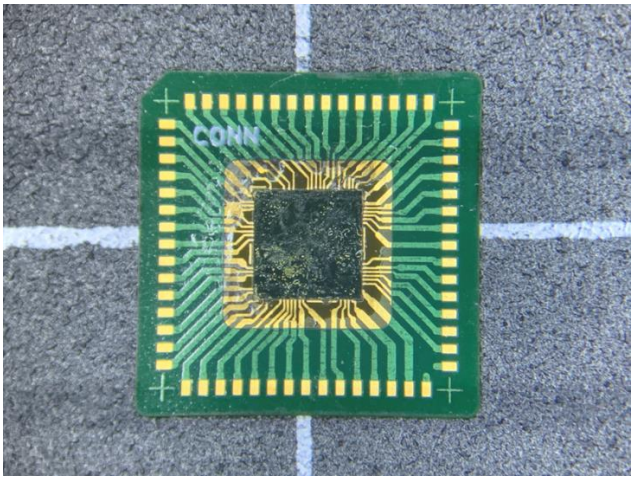


Fig. 6 - Flip-chip on flex hybrid FO module

Hi-Temp Test utilized 8 samples with Troom pre-test, 75C/24hr soak, 100C/24hr soak, 125C/24hr soak, Troom/72hr test, and 145C/24hr, test. High Temp Test Results at Troom, 75C/100C/125C/145C began with the identification of 6/352 pins failing for newly assembled devices. All pins were tested post temperature cycle and only 1/352 pins failed after temp with no new pins failing. The 101% post-test yield was determined to be healing of ACA interconnects when exposed to elevated temperature. This phenomena will be further evaluated as the ASI ACA flip-chip process continues to scale to higher pin count and smaller pitch.

IV. Conclusion

Because of the rapid advancements in integrated circuit manufacturing processes, P-CSP packaging solutions are becoming increasingly significant as they are required to provide reliability for continued chip thickness scaling.

SoP-TM is the first WLP process that provides full 6S protection without the added cost or complexity of die reconstitution.

The SoP process has been verified to provide high reliability for ultra-thin silicon. Mechanical testing, temperature testing and thin-silicon electrical testing validates the feasibility of SoP as a high-volume solution for P-WLCSP.

One of the primary elements driving demand for wafer level packaging technology over traditional packaging solutions is the growing demand for technical improvement in mobile devices that require small single die products. Moreover, one of the primary market drivers for wafer level packaging is the demand for faster, lighter, smaller, and more cost-effective high-performance packaging. SoP-TM is well engineered to meet market demands.

Acknowledgment

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