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Reliably Thin Electronics

iMAPS 2021

Advanced Protected Fan-In WLCSP

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Today's Presentation

1. A brief recap of CSP evolution and PSB
2. CSP FI, and FO and as a CSP process alternative
3. 2-side Protected WLCSP
4. 6-side Protected CSP (P-WLCSP)
    1. Thinnest fully protected CSP
    2. Lowest Cost fully protected CSP
5. P-WLCSP to SiP and the future

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Wafer Level Chip Scale Package - EVOLVED

- WLCSP
  - With the advent of bumped die, new IC packages evolved
  - Low IO WLCSP, High IO FC (flip chip), CBGA (ceramic ball grid array) and PBGA (plastic BGA)
  - Reliability for bumped die packages evolved differently for high and low IO bumped die

- Active side protection became important with the entry of high IO die
  - Bumps on traditional final passivation resulted in unacceptable reliability
  - Addressed with a BEOL (back end of line) FAB application of PSB (passivation stress buffer)
  - PSB was used earlier to protect molded die surfaces from the filler particles in the mold compound (filled epoxies) encapsulants in traditional plastic IC packages for WB (wire bond) devices
  - CBGA and PBGA packages also included encapsulants, including filled epoxies, to protect the rest of the die and the bumps to improve reliability

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WLCSP Fan-In

- Low IO WLCSP (aka Fan In) was built on wafers adding bumps and redistributing the pads as needed.
  - This resulted in the die being the package
  - However, without active side protection reliability issues ensued
  - To maintain wafer processing active side protection options were needed
  - One option was to build the components of a plastic package on the active side on the wafer
  - A simpler (lower cost) option was to use PSB as used on FC wafers for high IO BGA packages
  - The PSB approach provided acceptable performance, initially…

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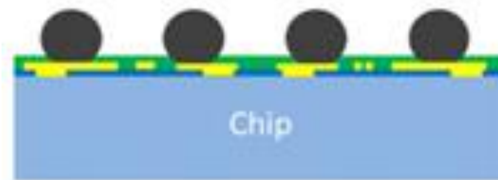
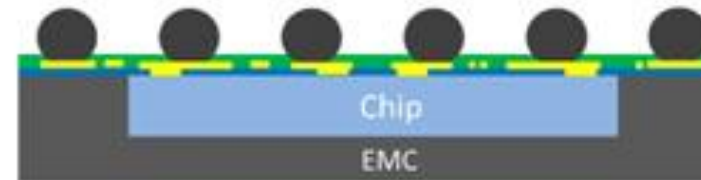
Evolutionary Problems

- As devices became more complex, reliability requirements increased
  - PSB based processes no longer provided the required reliability
  - Higher IO capability and better reliability evolved to non-WL CSP
  - Larger area was needed for bump distribution, as well as, additional protection for the rest of die



(a) WLCSP Packaging



(b) Fan-out Packaging

WLCSP vs CSP FO. Source: Semiconductor Engineering Aug. 19, 2021

- Small FO packaging processes were used to produce non-WL CSP
  - 6-side protected CSP (all 6 sides with similar material) was implemented using FO processes such as M-series
  - FO for CSP includes die reconstitution, expensive tapes, molding operations, etc.
  - Resolving the reliability issues of unprotected die justified non-WL CSP for FI, but the added cost and process complexity was and is far from optimal

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Back to WLCSP

- A lower cost alternative
  - Retain the simplicity of PSB WLCSP while encasing all sides of the die in a PSB like material replacing the encapsulate materials in the non-WL CSP options
  - This requires several changes to allow all side coverage of the device with PSB material which then acts as the encapsulate for the package
  - Emerging thin wafer processing facilitates the ability to provide protection to more than just the active side of the die
  - Earlier presentations and papers on Semiconductor-on-Polymer™ (SoP) reported how this can be done for protecting the top and bottom of the die to improve mechanical reliability, as well as die performance, versus single sided or unprotected thin die

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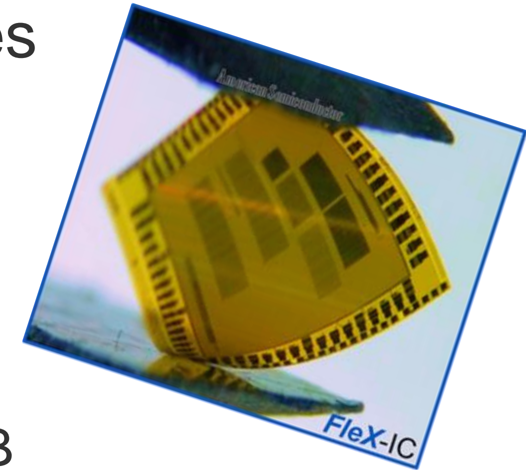
SoP WLCSP Packaging

- 2-side protected packaging was the first step toward fully protected WLCSP

- 2-side protected FleX-C SoP is one example
  - Produced excellent mechanical reliability for thin silicon devices
  - Developed to overcome the mechanical reliability and yield issues associated with thin die
  - Implemented frontside and backside polyimide layers
    - Reduced die edge chipping and cracking common to thin die
    - First introduced to the Flexible Hybrid Electronics (FHE) market for FCB
    - Achieved the primary FHE goal of maintaining the thinnest assemblies possible
    - Beyond FHE, the technology is being applied in chip-on-flex applications where previous SMT resulted in poor formats and reliability issues associated with flex deformations



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FleX-C™ 2-sided SoP™ WLCSP

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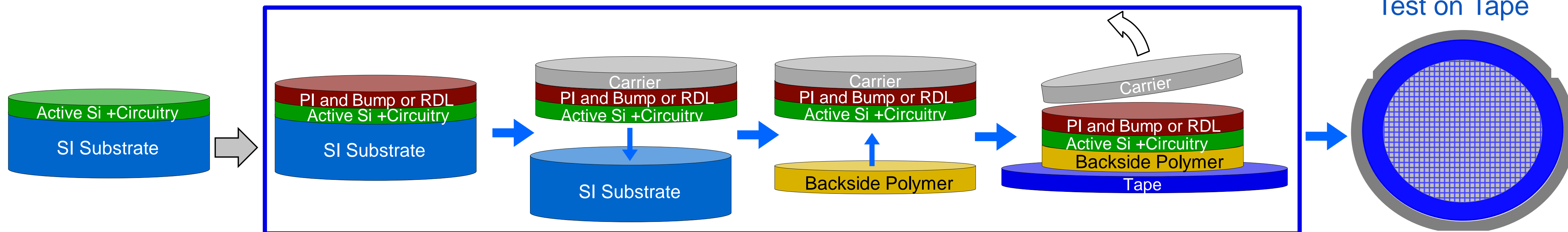

CMOS Wafer from any IDM or Foundry

Wafer Level Processing Technology

Temporary Carrier Bonding. Bulk Silicon removed (Silicon Substrate 10um)

Backside polymerization and stress balancing

SoP Wafer release and transfer to thermal Tape

Dicing on tape (High Speed Laser Dicing)

SoP ICs Tape on Frame, or Tape & Reel, Gel Pack, or similar

Source epak.com

- Compatible with Standard Wafer Level processing
- Thin Wafer Completely supported through module
- Technology optimized to ensure flat wafer processing
- **Produces the thinnest ICs in the industry**
- **Currently supporting FHE and chip-on-flex applications**

***No thin wafer** handling required in ultra-thin SoP process*

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SoP *FleX*-C Mechanical Reliability

Chip-on-flex Enablement

- Physical flexibility is maintained post assembly
- Eliminates flex shear problems
- Minimizes or eliminates mechanical failures at rigid/flex interfaces
- Demonstrated on PET, Paper and Cu-on-PI

Thinning Method	Total Thickness (um)	Die Size (mm)	RoC Fail (mm)	Failure mode
Conventional thinning	300	5.0 X 5.0	30	Delamination
		2.5 X 2.5	12	Delamination
	40	2.2 X 2.2	10	Delam & Cracking
	20	2.2 X 2.2	10	Delam & Cracking
SoP WLCSP	28um (Si<5um)	2.5 x 2.5	5	PASS

SoP on Pyralux® BLE flex demo

SoP on PET NFC flex demo

Radius of Curvature (RoC) Testing– ICs on flex

This work sponsored in part by the Air Force Research Laboratory AFRL/RX

Thinnest, Higher performance MultiChip Modules:

- Enhanced Thermal and Package uniformity
- Chip thickness matching using low cost polymer for improved multi-chip manufacturability
- Final Die-to-Die TTV performance < 2um

Thinning Method	Total Thickness (um)	Die Size (mm)	RoC Fail (mm)	Failure mode
Thin Die SOC	35 Si	2.16 X 2.28	10	Crack
SoP ADC	<5 Si	2.5 x 2.5	1	PASS (ASI)
SoP SOC	<15 Si	2.16 X 2.28	<5	PASS (Cypress)
SoP NFC	<15 Si	2.51 X 2.51	<5	PASS (NXP)
SoP RFID	<15 Si	1.66 X 2.05	<5	PASS (EM Micro)

***RoC – Radius of curvature bending

SoP enables Ultra thin flex assemblies with no impact on devices

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WLCSP Enabling RF Technology

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- SoP WLCSP may be most significant for RF devices that rely on SOI
  - The standard SoP process results in some amount of handle silicon remaining
    - The buried oxide/handle silicon interface is unchanged
    - Handle Si trap regions can be retained if desired.
    - However Rds can improve significantly with thinner handle silicon
  - SoP can be augmented for complete handle silicon removal
    - Eliminate substrate coupling capacitance
    - Low insertion loss backside PIs with Df < 0.003 @ 80 Ghz can be used
  - Additionally, the backside encasement can be selectively removed
    - Key areas to further eliminate parasitic issue
    - Heat sink application

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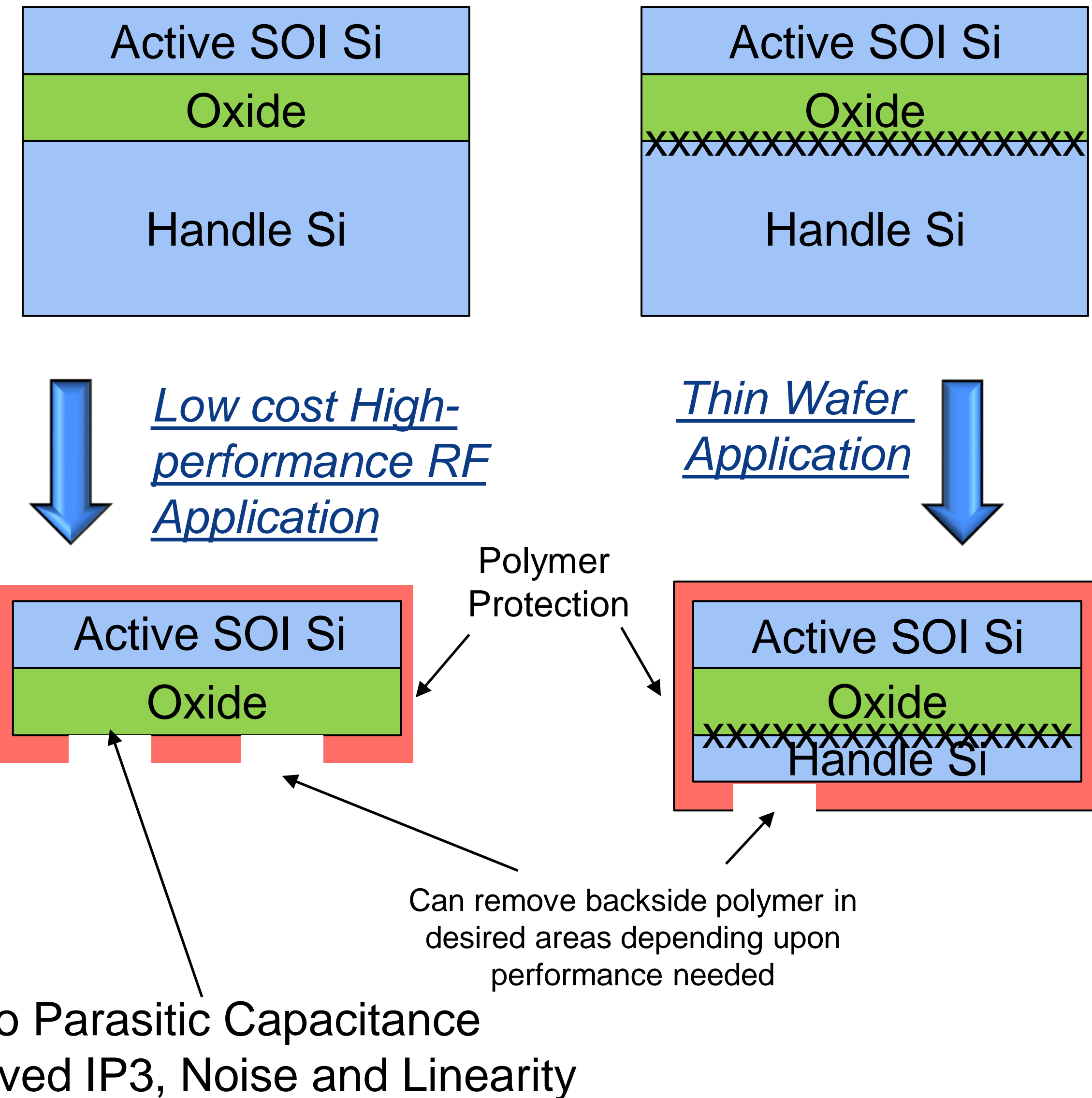
Silicon on Insulator – SoP options

- SoP process can be used on both Thin and Thick Film Silicon
  - Technology is independent of starting materials
- Can be used in two approaches depending upon need of device and application
  1. Thin Wafer Application
     - Ultra Thin applications – Standard process
     - Some amount of Silicon Handler wafer is still present
     - No need for redo of application circuits
  2. High performance RF Application - Elimination of Silicon Handling Wafer
     - No Substrate Coupling Capacitance
     - Low Insertion Loss backside PI available
       - Df < 0.003 @ 80 Ghz and higher
     - Handle Si trap region can be retained if desired
     - Polymer can be selectively removed in key areas of device eliminating any parasitic issue
     - Applicable for new designs or existing products



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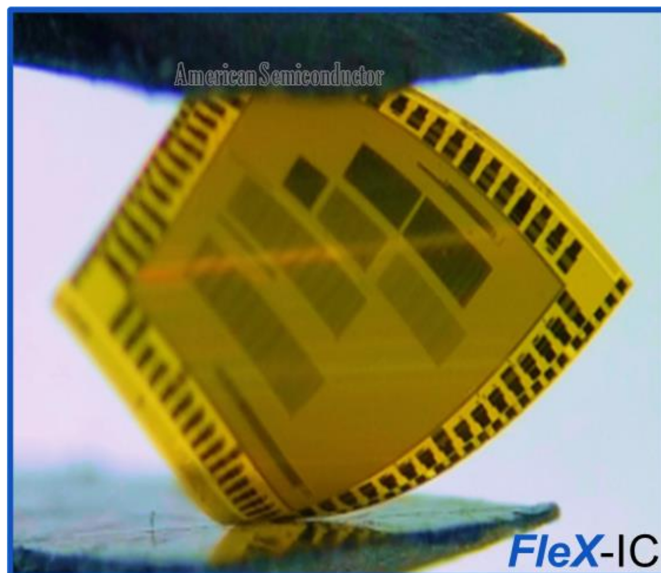
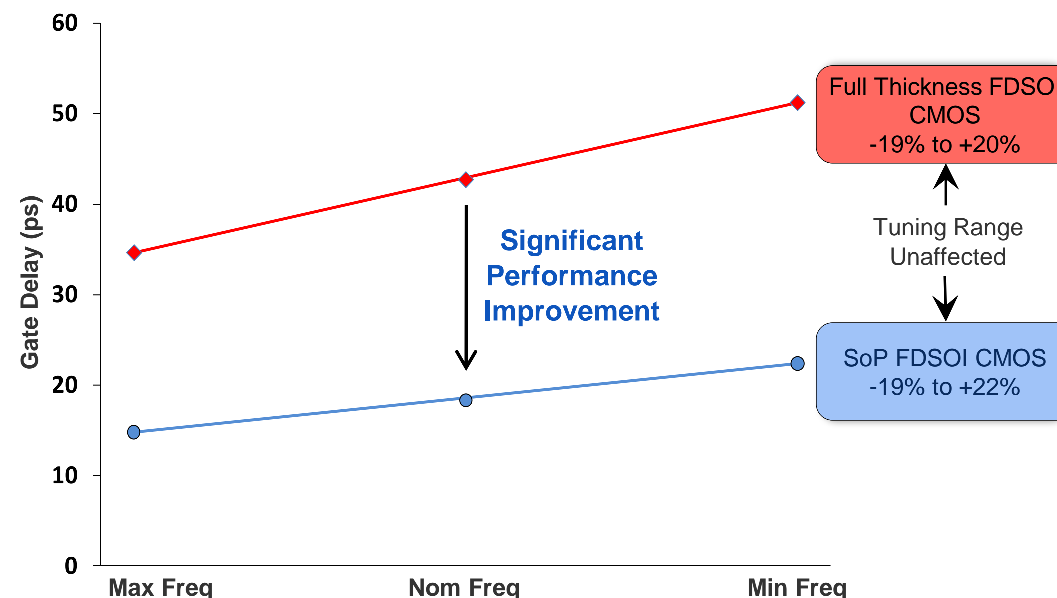
SoP for FDSOI

SoP FDSOI

- Handle Si fully removed
- Bottom junction capacitance eliminated
- Improved performance
- SOI thickness for sample: 2000Å



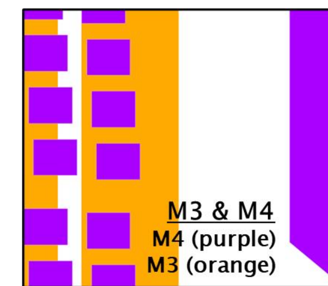
SoP FleX-C Packaged 130nm FDSOI CMOS



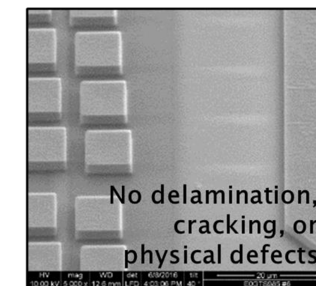
TESTING

HTOL 168 hours at 125C PASS
LTOL 168 at -25C PASS
ESD 4KV HBM PASS

Data Retention 150C non-bias PASS
Data Retention RoC PASS
Dynamic RoC >15k cycles PASS
Dynamic Torsion >90K cycles PASS



Layout View



SEM Analysis

Note: Preliminary SoP results for Jazz CS180 PDSOI shows improved Q for ring oscillators

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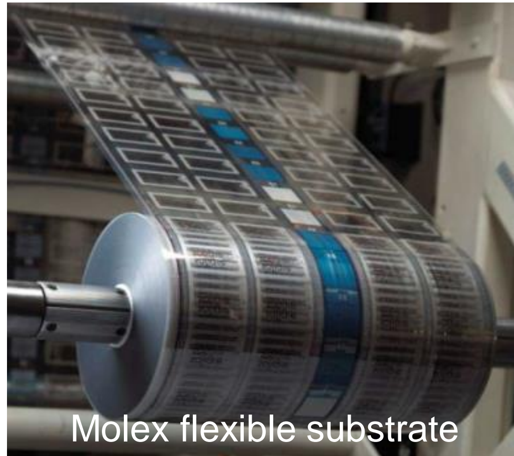
FHE = Flexible Hybrid Electronics

Flexible Hybrid System

"Combining thin FCB and flexible silicon-based ICs creates a new class of flexible electronics."

Flex or Printed Flexible Circuit Board (FCB)

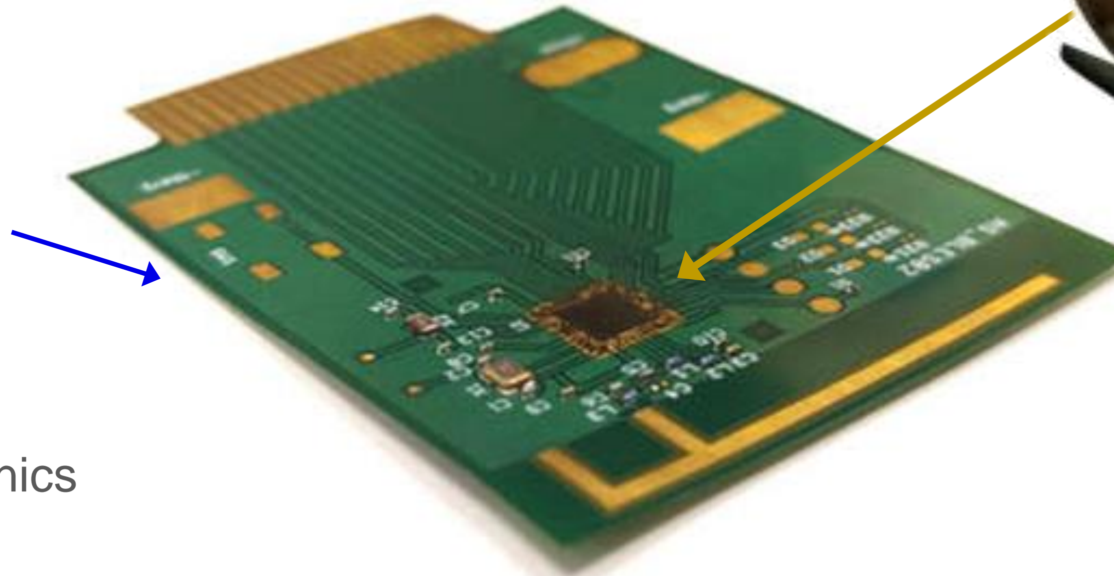
R2R, S2S, Large Format



Flex and Printed Electronics

- Sensors
- Interconnects
- Antennas
- Displays

- Low Cost, Large Format
- Roll-To-Roll, Screen, Inkjet Print, …

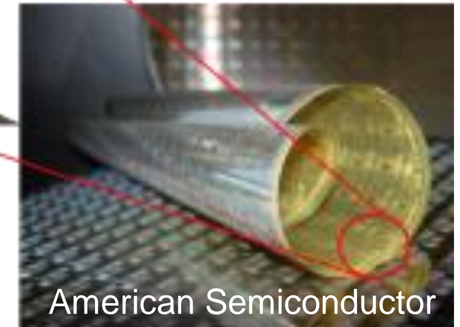


FleX-BLE Development Kit AS_DEVBLES02.kit

FHE enabling thinnerization

Ultra-thin SoP packaged *FleX*-ICs

High Performance, High Density



FleX-ICs

- Bluetooth® SOC
- Data Processing
- Data Storage
- Communications
- Low Cost, High Performance
- ***FleX*** is a Semiconductor-on-Polymer (SoP) **chip scale packaging (CSP)** process.

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6-side protection: P-WLCSP

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- "Protected WLCSP" or P-WLCSP
  - 6-side protection without the cost and complexity on non-WL FO type processes
  - P-WLCSP does not require pre-package die thinning, dicing or reconstitution
  - P-WLCSP Substantially reduce the equipment and process steps required for processing
  - Material reductions with the elimination of dicing tape and molding materials
- FleX-TM™ is a new SoP 6-side protected P-WLCSP process
  - Full protection, without the cost/complexity of non-WL FO processes used for protected CSP FI
  - 300mm process utilizes polyimide for encasement
  - The process includes maskless processing and high temperature temporary bonding
  - Enables use of a wide selection of PI for stress balancing
  - Final singulation (dicing) speed enhancement due to P-WLCSP PI scribe streets
- Enabling ultra-thin devices
  - Reduced die thickness improves capability for through silicon via (TSV) size and pitch
  - Enables high-temperature backside RDL (B-RDL) and heat sinks
  - CMOS silicon thicknesses is typically 10-15um, but can be adjusted as needed
  - SoP processing on SOI has demonstrated Si Tx at 2000A with SOI speed improvement

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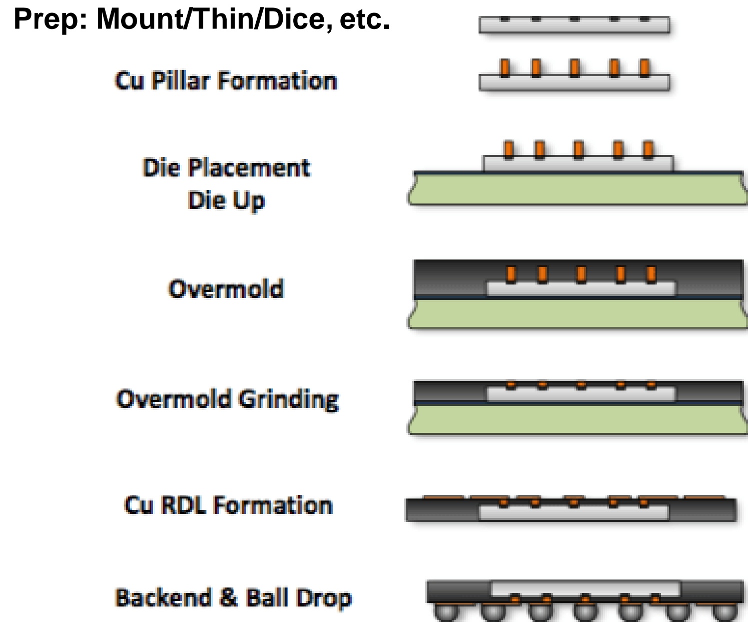
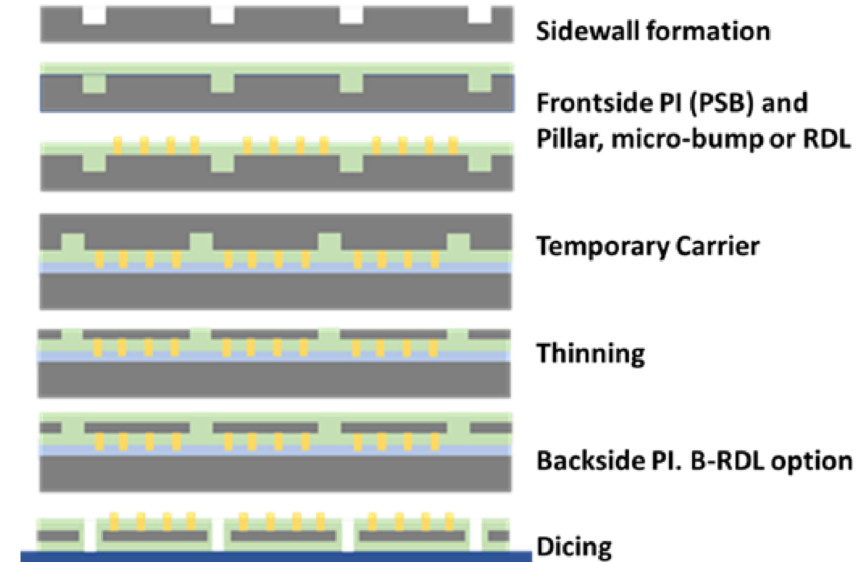
P-WLCSP vs non-WL CSP

- Comparison of non-WL CSP and P-WLCSP SoP process provides an understanding of cost and complexity of protected packaging technology.



M-Series CSP FO Process. Source: SemicondcutorEngineering Feb. 2018



FleX-TM Protected WLCSP, U.S. Patent 9,082,881

- P-WLCSP processing provides cost reduction and performance improvement in CSP FI applications
- Produce robust ultra-thin devices for SiP applications - chiplets and heterogeneous integration
- Higher pin-counts and thinner board assemblies are macrotrends in modern electronics
- Reducing layer thicknesses, along with the opportunity to connect on top and bottom of die without any significant cost penalty is significant.

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FleX-TM 6-side protected SoP WLCSP

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300mm Wafer

Cross Section

Si Test Die

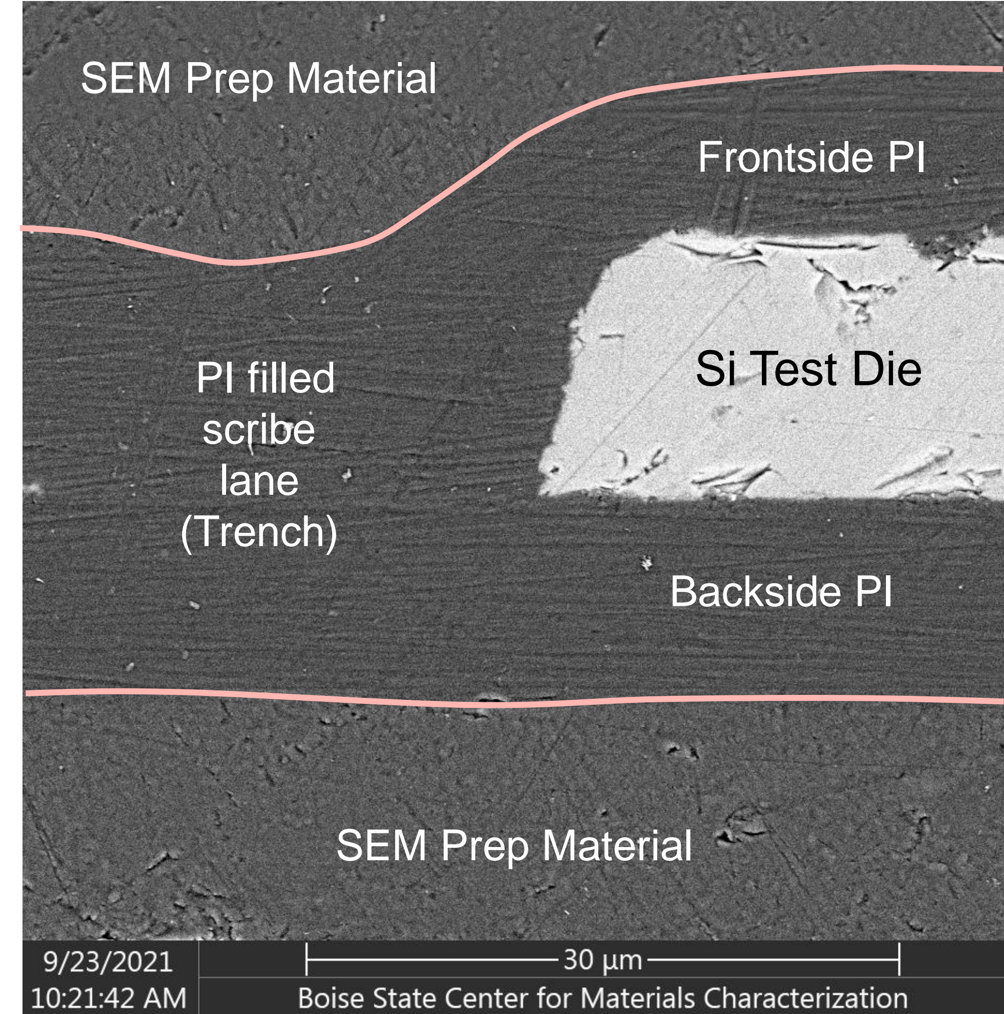
Si Test Die

PI filled Scribe Lane

Si Test Die

PI filled Scribe Lane

Si Test Die



Trench 45um
Frontside PI 10um
Silicon 11um
Backside PI 10um
Sidewall PI ~10um

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FleX-TM Summary

SoP reduces processing steps and material usage for protected fan-in

- True wafer level CSP process (WLCSP) eliminates pre-packaging wafer prep:
  - No pre-package wafer grind
  - No pre-package dicing tape
  - No pre-package singulation
  - No pick-and-place for reconstitution
- Die reconstitution eliminated
- Maskless PSG
- Only 1 thinning step required – utilizes clean dry release temporary adhesive
- Low cost reusable silicon carrier wafer
- Only 1 singulation step required
- Only 1 tape layer
- Standard wafer level processing for bumps, pillars and/or RDL
- Overmold process eliminated

50% fewer steps –> 50% less capital, or 2X capacity increase

50% Less labor cost –> Cycletime 50% less, improves cash flow

30-50% Less material cost

SoP – Lowest Cost Protected Fan-In

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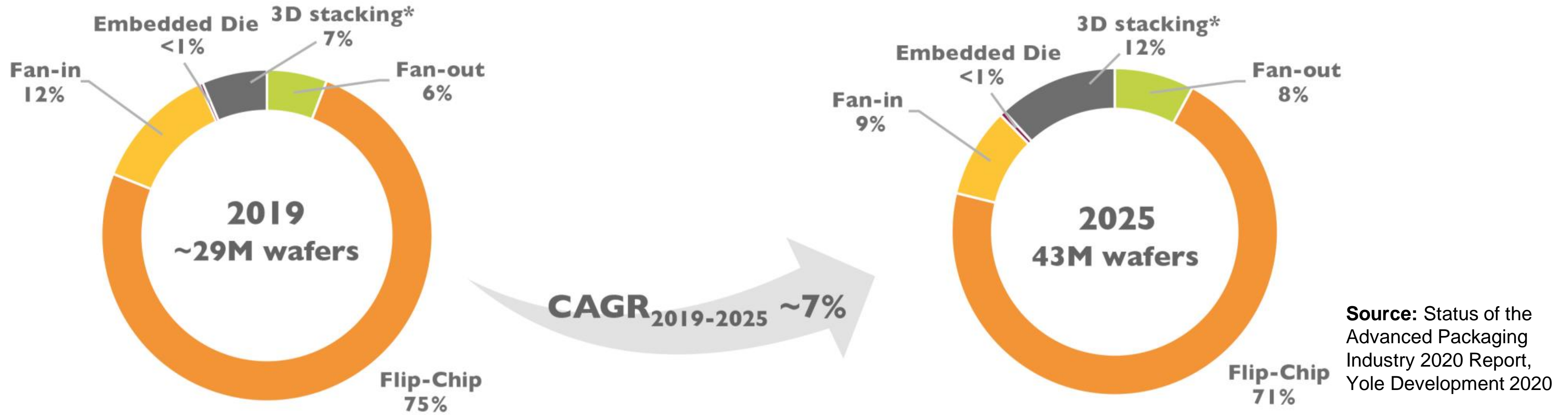
Direction for SoP FleX-TM: $2B TAM -> $36B by 2025

Market Forecasts



Source: Status of the Advanced Packaging Industry 2020 Report, Yole Development 2020

2019-2025 WLCSP/Fan-In package revenue evolution $2B 2019- $2.5B 2025 – Yole Development Nov. 2020

Advanced Packaging $25.6B expected to reach $36.3B by 2025, CAGR 7. 8% – Yole Development Dec. 2020

Heterogeneous Integration projected to grow to 54 billion packages by 2025 – IMAPS/TechSearch Mar. 2021

Packages using chiplets expected to show a CAGR of 104% from 2020 to 2025 – IMAPS/TechSearch Mar. 2021

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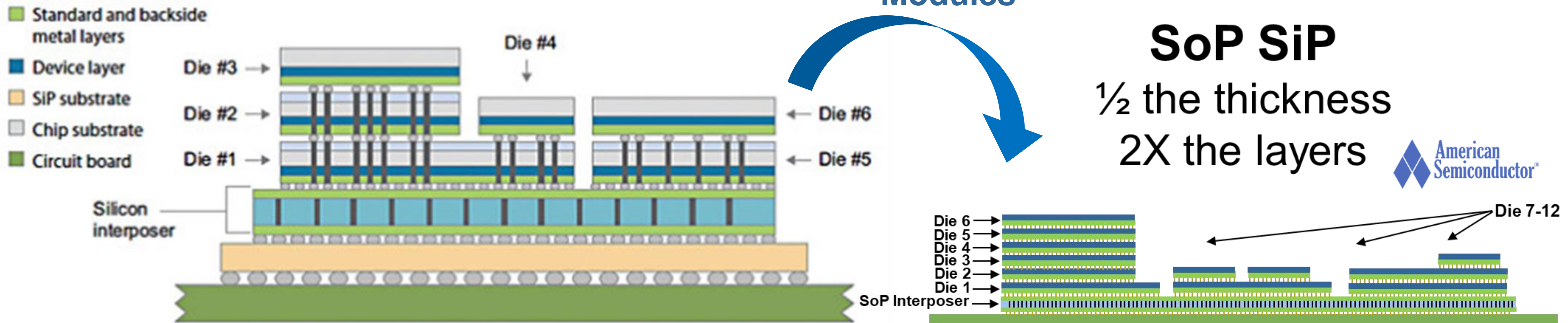
Vision for P-WLCSP Advanced Packaging



Source: Tech Design Forum May 8,2018

- Thin, protected, ICs (SoP)
- Fully protected CSP for high yield
- Device performance improvements
- Thinner, finer pitch interposers
- High density TSV
- Direct Interconnect

- Added IC count without larger package
- Multi-function modules
- Sensor and Passive device integration
- Wireless
- Maskless
- Highest value add

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Conclusion

- Full die protection has been widely adopted for reliability in FO, but with a high cost
- P-WLSCP SoP provides full die protection AND retains the simplicity of WLCSP with low cost
- FleX-TM SoP includes similar material on all 6 sides, minimizing uneven stress on the die
  - Reliability
  - Performance
- Continued P-WLCSP progress relies on further package reliability testing
- The next step requires collaboration with device manufactures and technology adopters
  - IDMs
  - Fabless
  - EDS
- FO processes bridged the reliability gap for CSP FI, P-WLCSP is proposed as the approach that will provide the die level building blocks needed for advanced multi-chip packaging solutions

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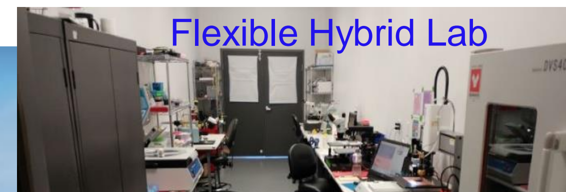
American Semiconductor - Boise, Idaho

American Semiconductor is the industry leader in ultra-thin advanced packaging. We develop state-of-the-art ultra-thin electronics technology.

- Founded Nov. 2001
- Over 21 SBIR wins
- 2-time Boeing SOTY

Member:



Commercializing Semiconductor-on-Polymer™ (SoP™) technology for dual-use production

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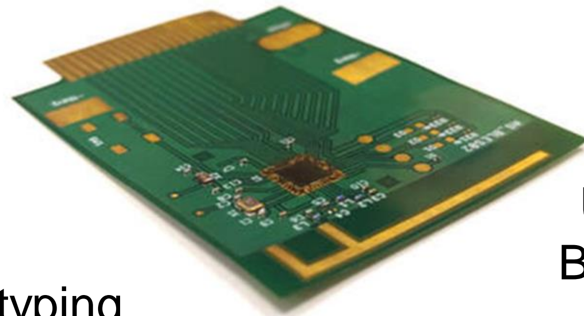
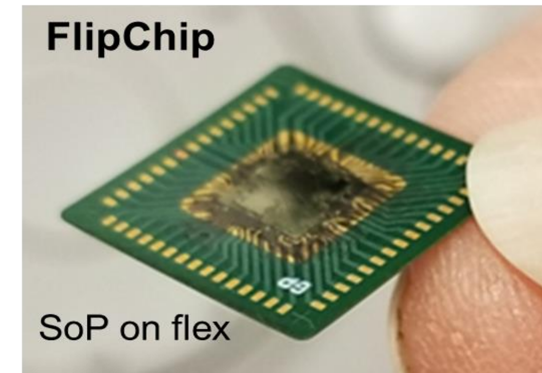
Technology Commercially Available



Ultra-thin Bluetooth®

SoP Chips for prototyping



Product	Description
AS_ADC100x	FleX-ADC Analog-to-Digital Converter: 8-channels, 8-bits ASI (TowerJazz Semiconductor Foundry)
AS_ADC2001	FleX-ADC Analog-to-Digital Converter with 3 Configurable Op Amps ASI (TowerJazz Semiconductor Foundry)
AS_CY820x	FleX-SoC (System-on-a-Chip) with Capacitive Sense Cypress Semiconductor PSOC® CY8C20XX6A/S
AS_EM4325P	FleX-RFID 900MHz RFID Communication Temperature Monitoring IC EM Microelectronics EM4325
AS_NHS3100P	FleX-NFC Temp Logging IC with ARM® Cortex-M0+ NXP Semiconductor NTAG SmartSensor with Temperature Sensor
AS_AM39513	FleX-NFC Sensor Tag IC AMS (Austria Microsystems) AS39513 NFC Sensor Tag IC
AS_OPA4002	FleX-OpAmp Quad High Performance Op Amps ASI (TowerJazz Semiconductor Foundry)
AS_OPA4003	FleX-OpAmp Quad Output Transconductance Op Amps ASI (TowerJazz Semiconductor Foundry)
AS_CY8C424	FleX-BLE Bluetooth Low Energy with ARM® Cortex-M0 Cypress Semiconductor PSOC® 4 Bluetooth LE
AS_NRF51822	FleX-BLE Bluetooth Low Energy with ARM® Cortex-M0 Nordic Semiconductor nRF51822
Customer SoP	**Additional customer specific wafers are being packaged in SoP CSP**

SoP NFC Chips and Assemblies

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Thank You

SoP packaging supported in part through
Joint Development with HD MicroSystems

Special thanks to Disco for their on-going
support of special processing requirements

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