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Reliably Thin Electronics

oe-a
End-user Workshop hosted by Meta

June 30, 2022

Advanced IC Packaging and Assembly for AR/VR

1. Requirements for next generation AR VR Headsets
2. IC packaging necessary to meet next generation form factors
3. Reliability and application of advanced packaging

Doug Hackler
American Semiconductor

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AR/VR

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Source: Walmart

Source: tomsguide

Source: BuyersGuide

Source: Amazon

Source: Extremetech

Source: Amazon

Source: GameStop

Source: Amazon

Source: Amazon

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What do they all have in common?

1. Must be compatible with VR/AR wearable applications
    1. Need to integrate seamlessly into VR/AR applications
    2. Durability must provide use specific environment reliability
2. Require comfort “wearability” for the user
    1. Increasing VR/AR durations-of-use drive need for comfort (flexible/stretchable)
    2. Thin, conformal, light weight (fashionable)
3. All use integrated microchips
    1. Sensors
    2. Data processing and memory
    3. Wireless Communication

They all rely on conventional electronics that are often too big, too bulky, uncomfortable or even sources of adverse reactions (nausea, eye strain, etc.)

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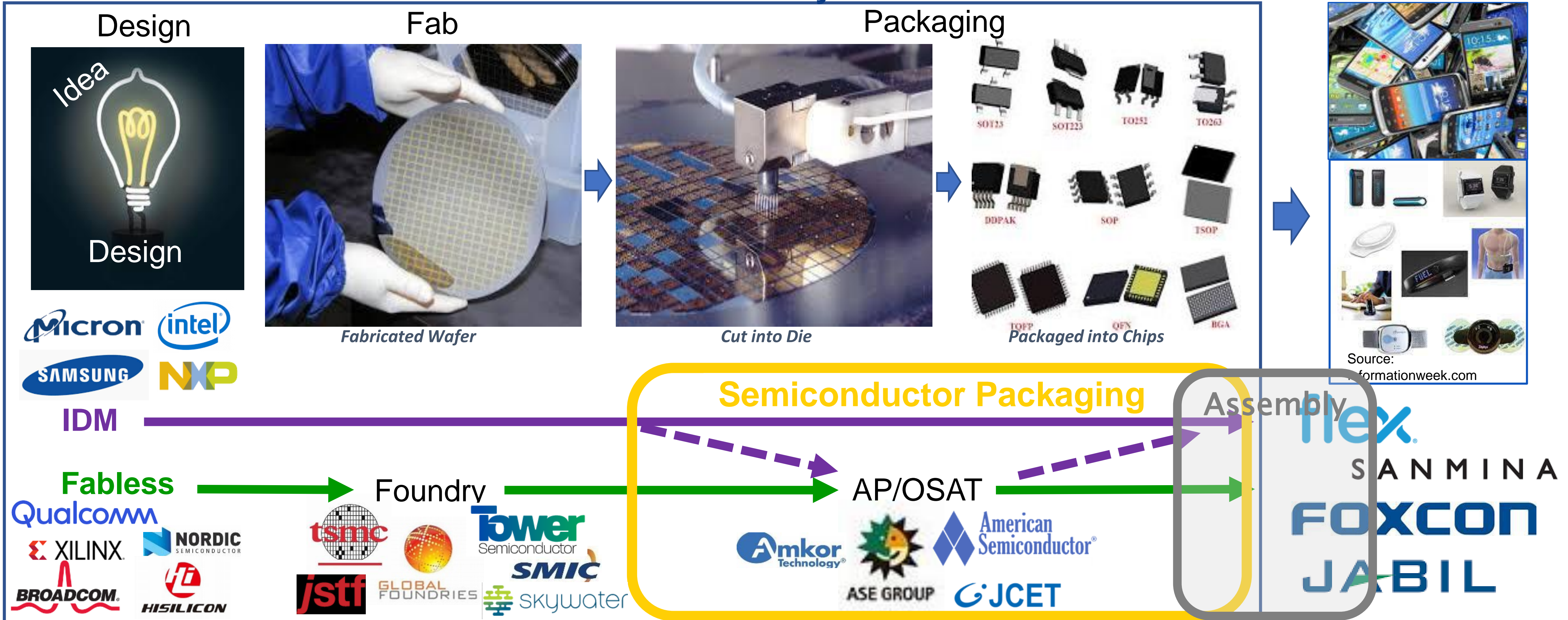
Advanced Packaging and Assembly can provide product form factors needed to address the limitation and inadequacies of current microelectronics



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Enabling Packaging and Assembly Technology

1. Thin and ultra-thin IC Packages
    1. Low profile
    2. Flexible
    3. Alternative encasement materials
2. Chip on flex Assembly
    1. SiP, AiP, sensors, power
    2. Thin and flexible
    3. Stretchable
    4. New reliability options
3. Next generation – Smart Interposer/Substrate/FCB
    1. Multichip
    2. WLCSP

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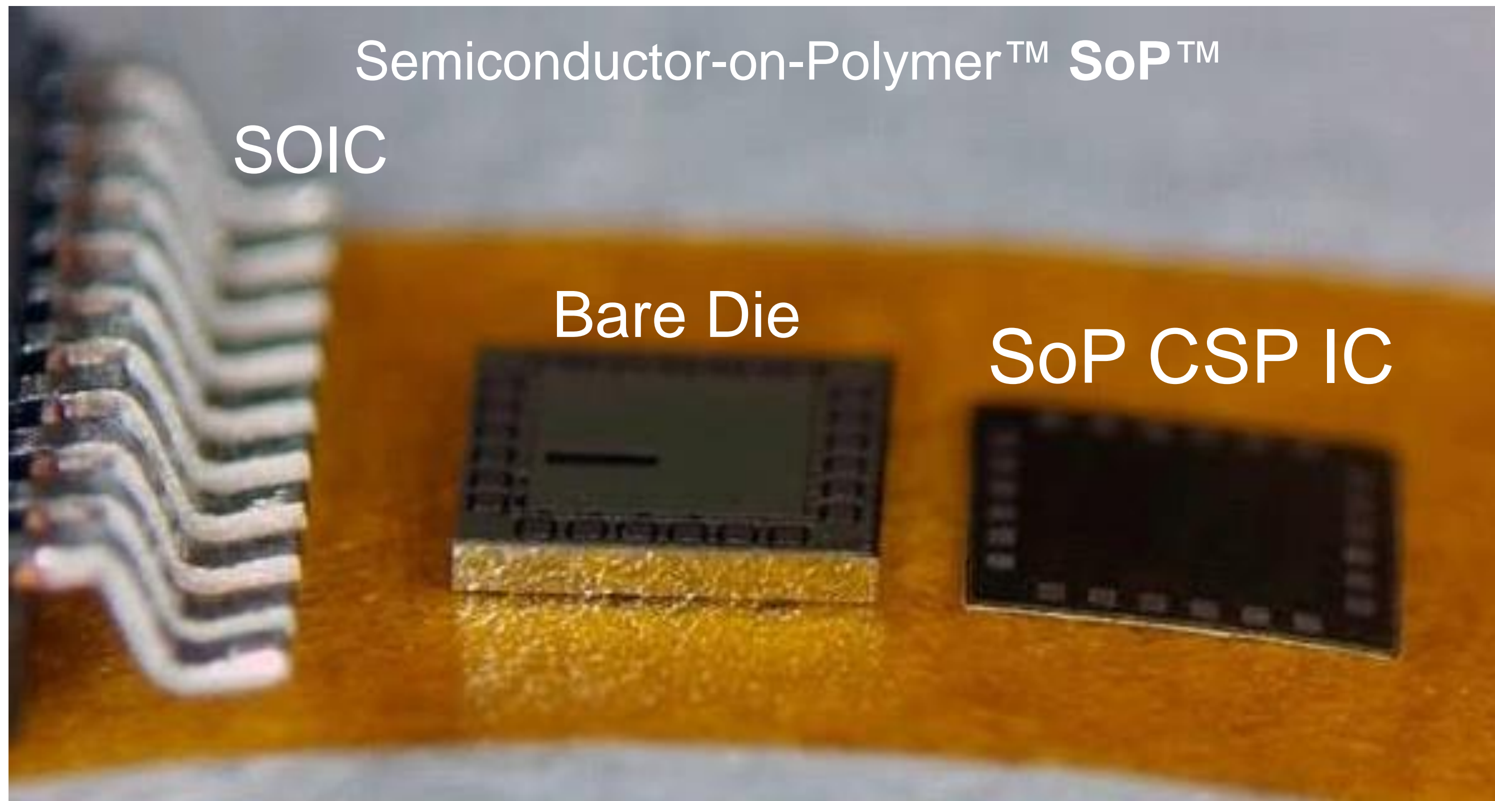
Thin IC Packaging

First introduced as FleX-C 2-side protected ultra-thin and flexible package for CMOS ICs



SoP P-WLCSP technology makes the ***thinnest chips possible***

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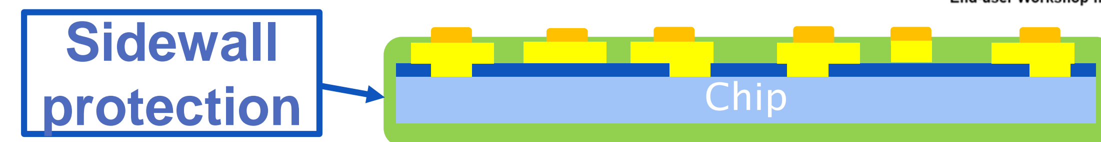
Today: SoP-TM™ Fully Protected Ultra-thin ICs

SoP for 6-sided (6S) protected fan-in



SoP (6S) P-WLCSP

- True wafer level CSP process (WLCSP) eliminates pre-packaging wafer prep:
  - No pre-package wafer grind
  - No pre-package singulation
  - No pre-package dicing tape
  - No pick-and-place for reconstitution
- Maskless PSG
- Only 1 thinning step required – utilizes clean dry release temporary adhesive
- Low cost reusable silicon carrier wafer
- Only 1 singulation step required
- Only 1 tape layer
- Standard wafer level processing for bumps, pillars and/or RDL
- Overmold process eliminated

50% fewer steps –> 50% less capital, or 2X capacity increased for existing facilities

50% Less labor cost –> Cycletime 50% less, improves cash flow

30-50% Less material cost

SoP – Lowest Cost Protected Fan-In

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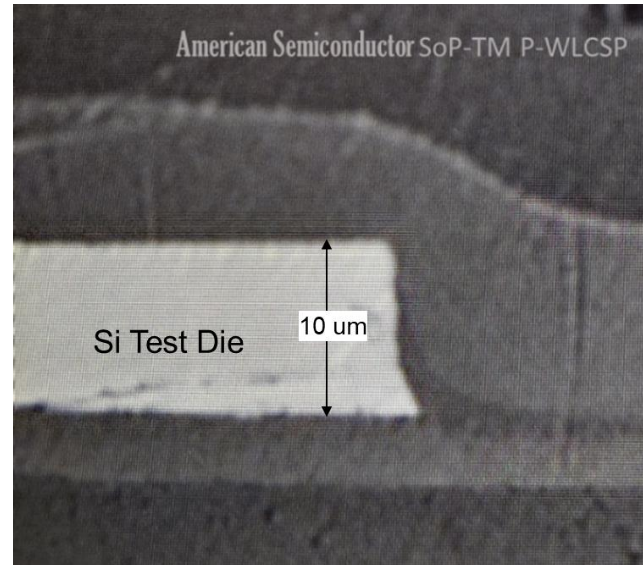
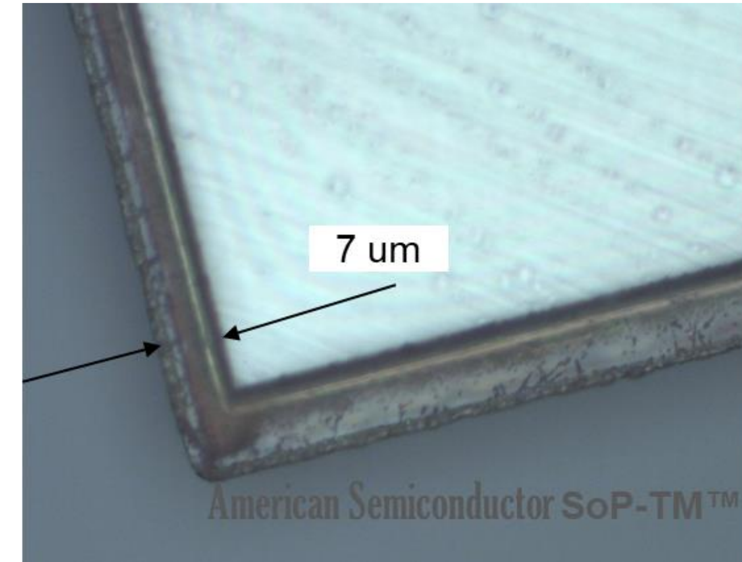
SoP-TM: 6-side die protection

DPC2022 SoP-TM development update

Current progress for SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection
Improved sidewall formation and demonstration of laser singulation

Trench 45um
Top PI (PSB) 10um
Silicon 10um
Bottom PI (PSB) 4um
Sidewall PI (PSB) ~7um





- Full 6-side protection
- Adaptive patterning enables use of encasement materials
- Applicable to any IDM or Fabless Manufacturer IC

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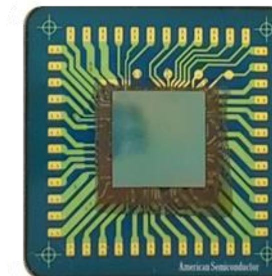
Assembly: FleX-on-flex™ Direct Interconnect

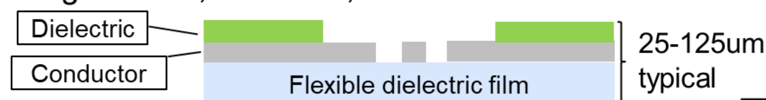
SoP FleX die assembly

- Direct Interconnect is used to simultaneously complete die attach and die interconnect
- ACA eliminates the need for underfill
- Flex-on-flex assemblies can run through standard lamination to add overcoats
- ACA flip-chip is compatible with standard SMT processing
- ASI maintains in-house assembly capability for ACA flip-chip manufacturing



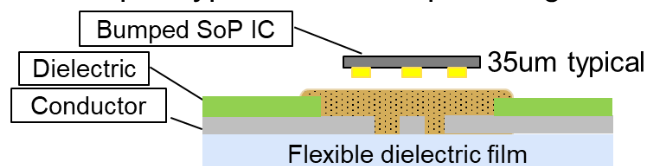
High pin count ACA flip-chip assembly

1. Circuit on flexible circuit board (FCB)
   Ag-on-PET, Cu-on-PI, etc.

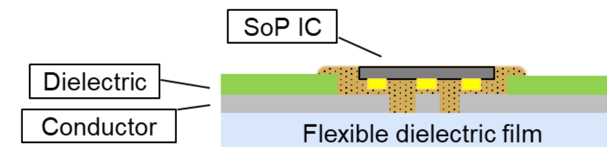


2. Add connective material
   ACA, ACF, Solder, etc.

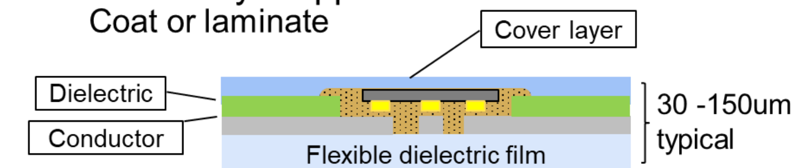
3. Flip-chip SoP IC placement
   2-100 pad typical at 100um pitch or greater



4. Flip-chip SoP IC Bonding
   2-100 pad typical at 100um pitch or greater



5. Cover Layer applied
   Coat or laminate



FHE System
Ultra-thin, physically flexible.

6. Ready for conformal surface mounting, molding, etc.

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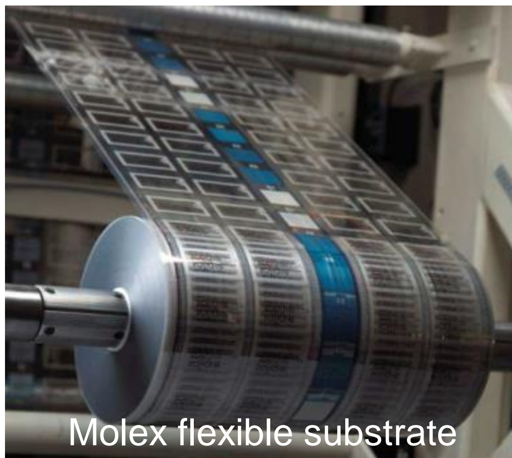
Flexible Hybrid System

"Combining thin FCB and flexible silicon-based ICs creates a new class of flexible electronics."

Flex or Printed Flexible Circuit Board (FCB)

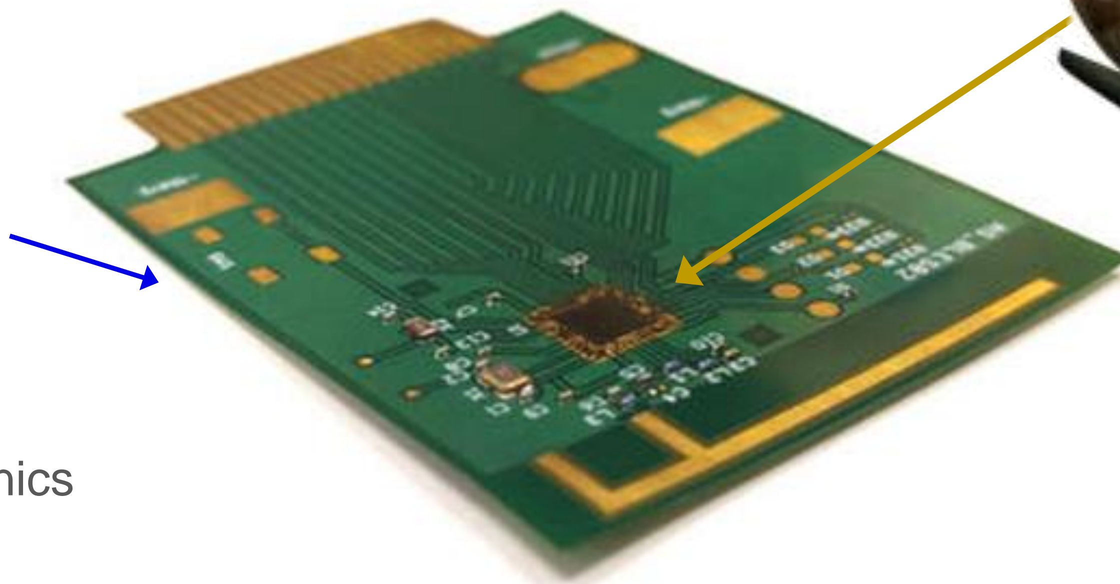
R2R, S2S, Large Format



Flex and Printed Electronics

- Sensors
- Interconnects
- Antennas
- Displays

- Low Cost, Large Format
- Roll-To-Roll, Screen, Inkjet Print, …

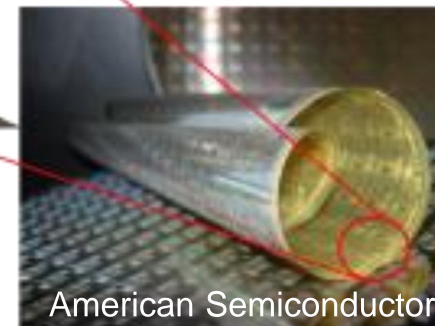


FleX-BLE Development Kit AS_DEVBLES02.kit

FHE enabling thinnerization

Ultra-thin SoP packaged *FleX*-ICs

High Performance, High Density



FleX-ICs

- Bluetooth® SOC
- Data Processing
- Data Storage
- Communications
- Low Cost, High Performance
- *FleX* is a Semiconductor-on-Polymer (SoP) **chip scale packaging (CSP)** process.

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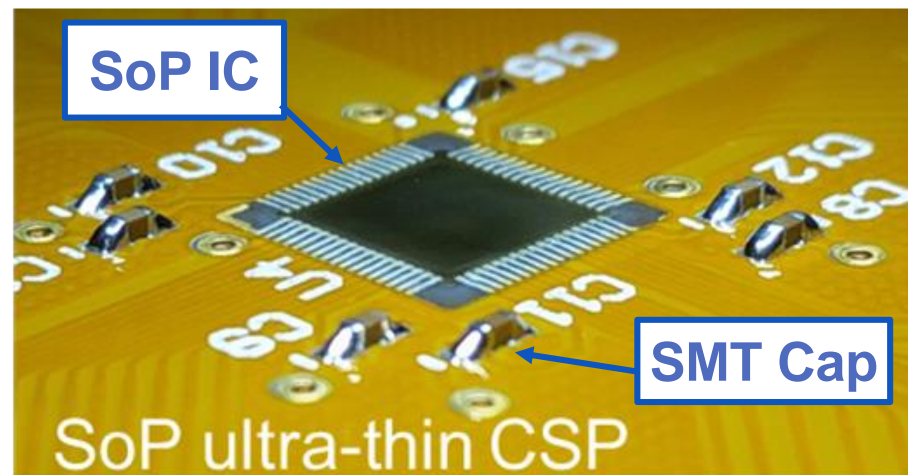
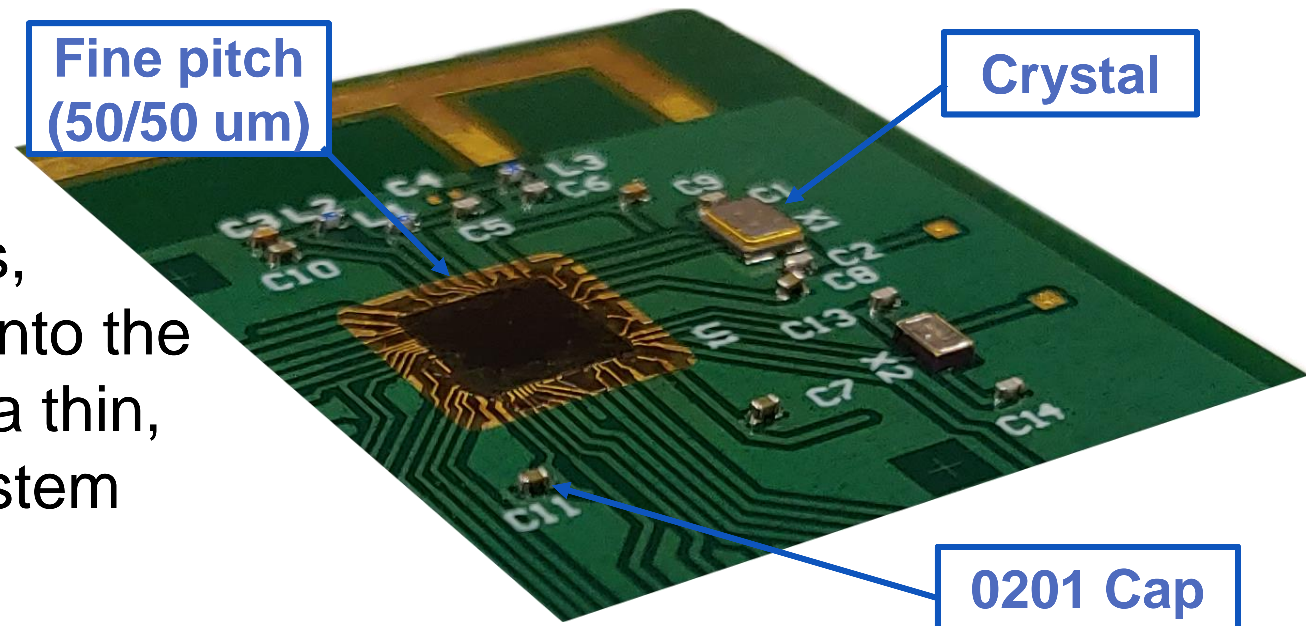
What's next? SoP Smart Interposer/Substrate/FCB

1. SoP resolves thickness and conformability issues associated with IC assembly
2. SOTA chip-on-flex assembly today relies on SMT of the smallest devices possible for resistors, capacitors and crystals
   a) 0201 and 01005 are typical
   b) Crystals
   c) MEMS sensors
3. Smart interposers integrate resistors, capacitors and fine pitch interfaces into the Interposer/Substrate/FCB to create a thin, flat, flexible and easily laminated system





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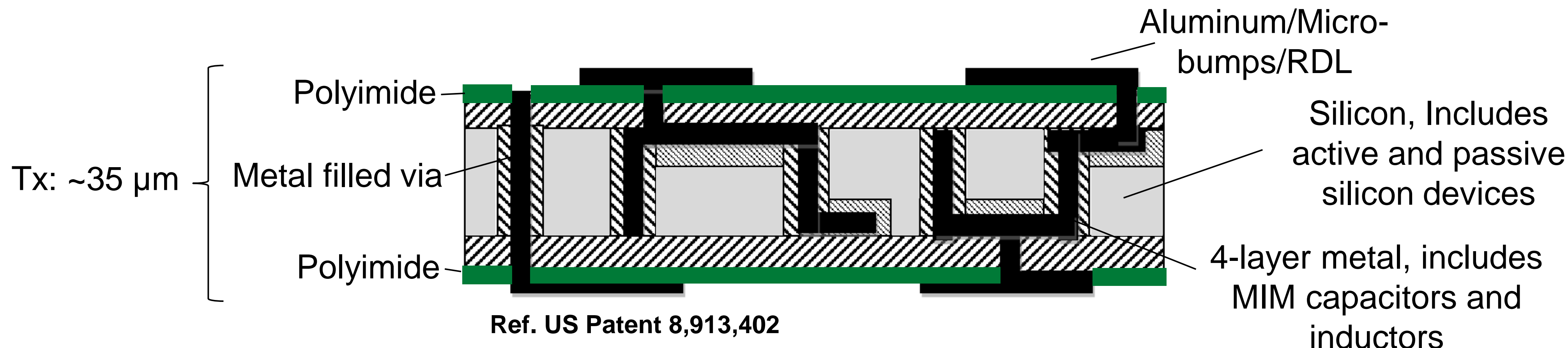
What's next? SoP Smart Interposer/Substrate/FCB

SoP Si Interposers are a "Smart-Interposer" technology



Ref. US Patent 8,913,402

- FEOL fabricated as an integrated circuit itself using readily available foundry process
- BEOL fabricated in SoP for ultra-thin and flexible capability, and backside features
- Includes precision resistors, capacitors, inductors
- Capable of including flexible photonic silicon waveguides (US Patent 9,733,428)
- High Density Interconnections between stacked metal layers
- Precise dimension tolerances ease IC bonding and connection
- Semiconductor materials match CTE of silicon ICs
- High density interconnections on both top and bottom surfaces

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SoP-TM First Mechanical Test

Dynamic Bend Test

- ASI TEST003 derived from ASTM D522-93a
- Chips mounted on flex coupons of PET or PI
- Robotic cycling at specific (RoC) for bend and release in concave and convex orientation
- Test: 10mm RoC, 10,000 cycles

Static RoC Testing

- SoP-TM Test Chip, no coupon
- Manual conformance to RoC mandrel

SoP-TM Mechanical Reliability

Test	Concave	Convex	
ASI TEST003 10mm, 10,000 cycles	PASS	PASS	SoP- TM, ACA FC on PET
Static RoC 12 mm	PASS	PASS	SoP-TM only
Static RoC 10 mm	PASS	PASS	SoP-TM only
Static RoC 8 mm	PASS	PASS	SoP-TM only
Static RoC 7 mm	PASS	PASS	SoP-TM only
Static RoC 6 mm	PASS	PASS	SoP-TM only
Static RoC 5 mm	PASS	PASS	SoP-TM only
Static RoC 4 mm	PASS	PASS	SoP-TM only
Static RoC 3 mm	PASS	PASS	SoP-TM only
Static RoC 2.5 mm	PASS	PASS	SoP-TM only
Static RoC 2 mm	PASS	PASS	SoP-TM only
Static RoC 1.5 mm	Cracked	Cracked	SoP-TM only

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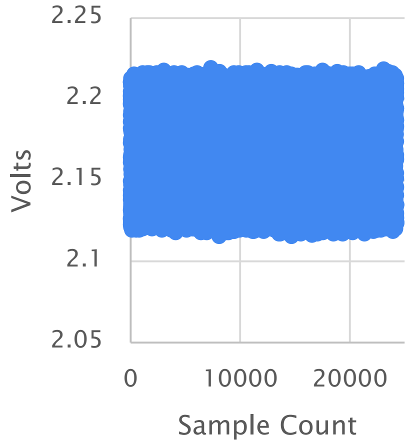
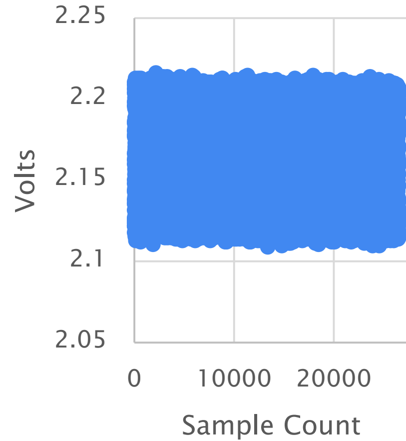
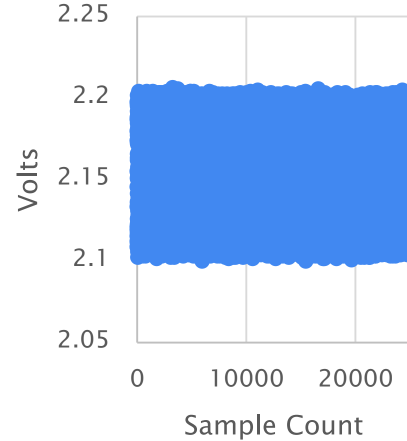
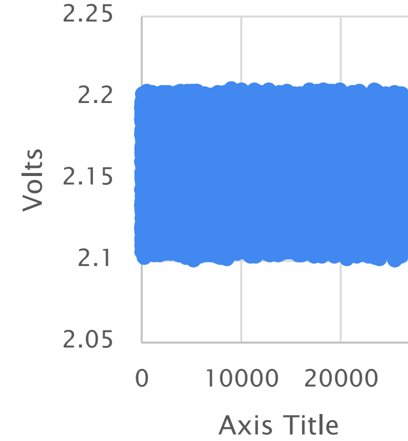
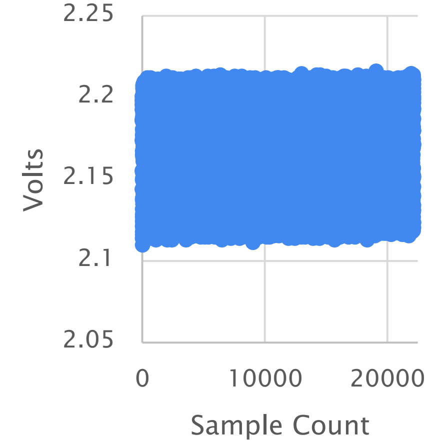
Static Bend Test Vdd Result











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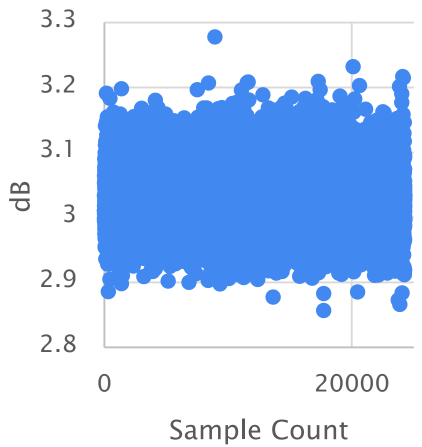
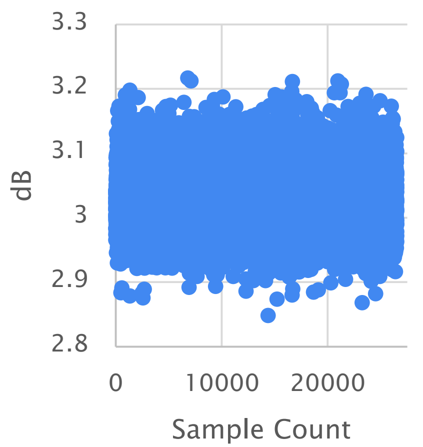
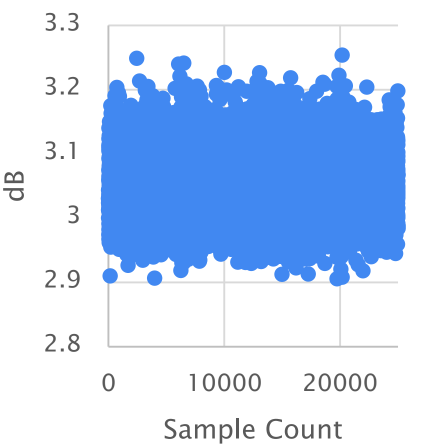
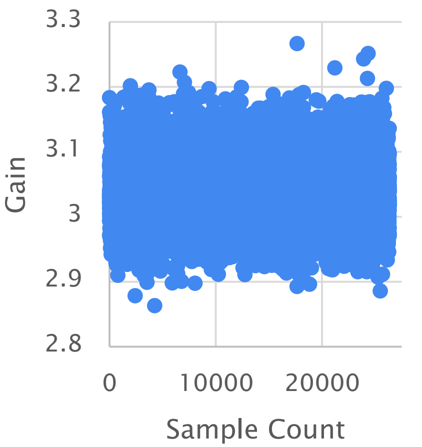
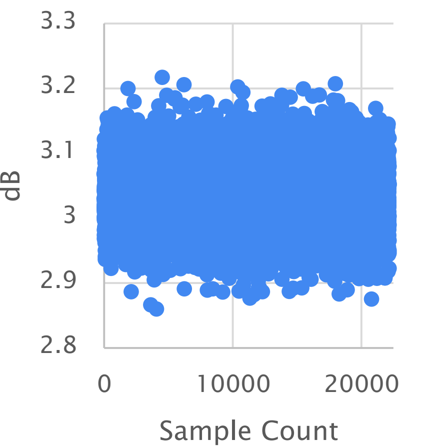
Static Bend Test Gain Result











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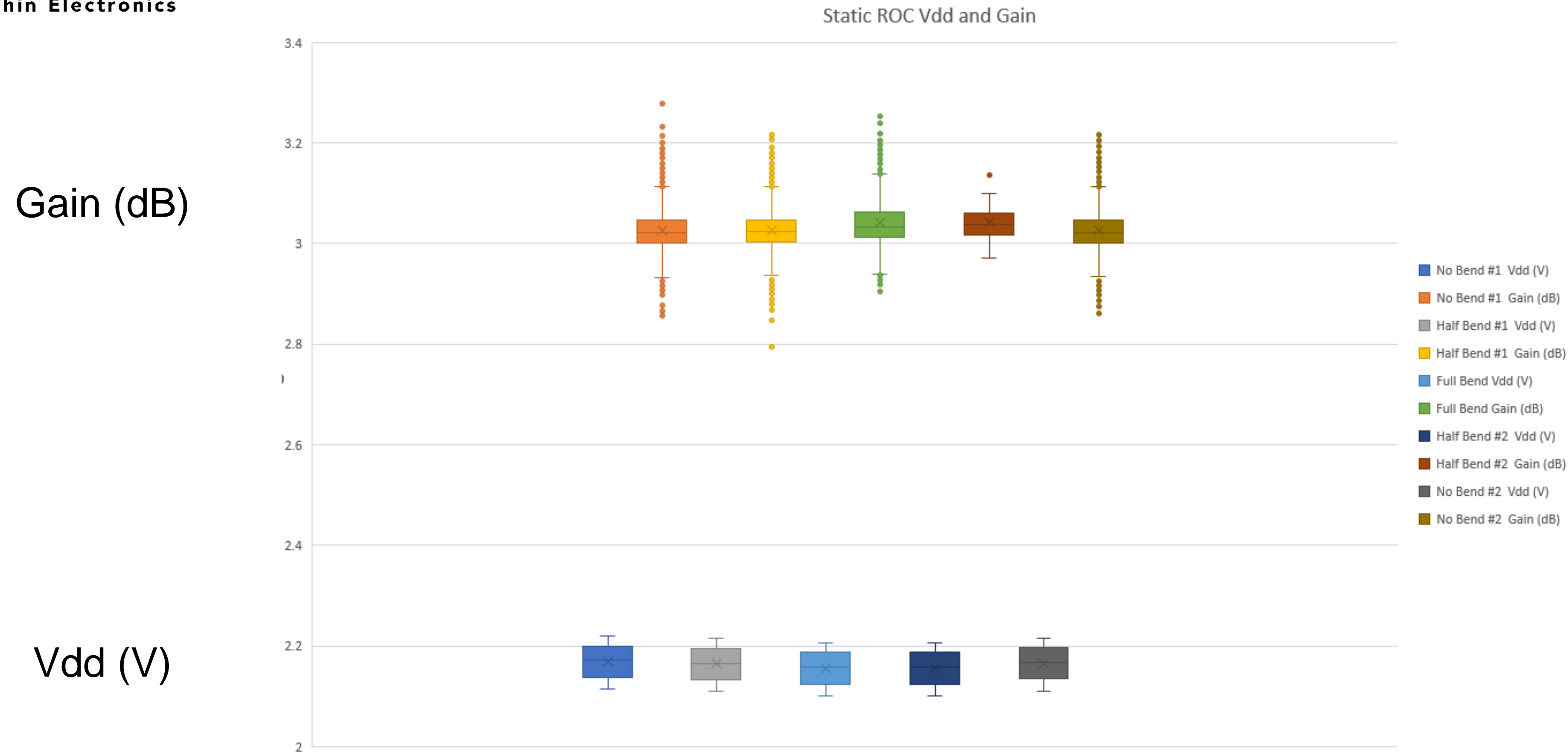
Static RoC Summary Statistics

Box Plot



- Static RoC OpAmp test used sample after 10k concave + 10k convex cycles at 10mm RoC
- Vdd difference between no bend and full bend only 0.013V
- Gain difference between no bend and full bend only 0.016dB

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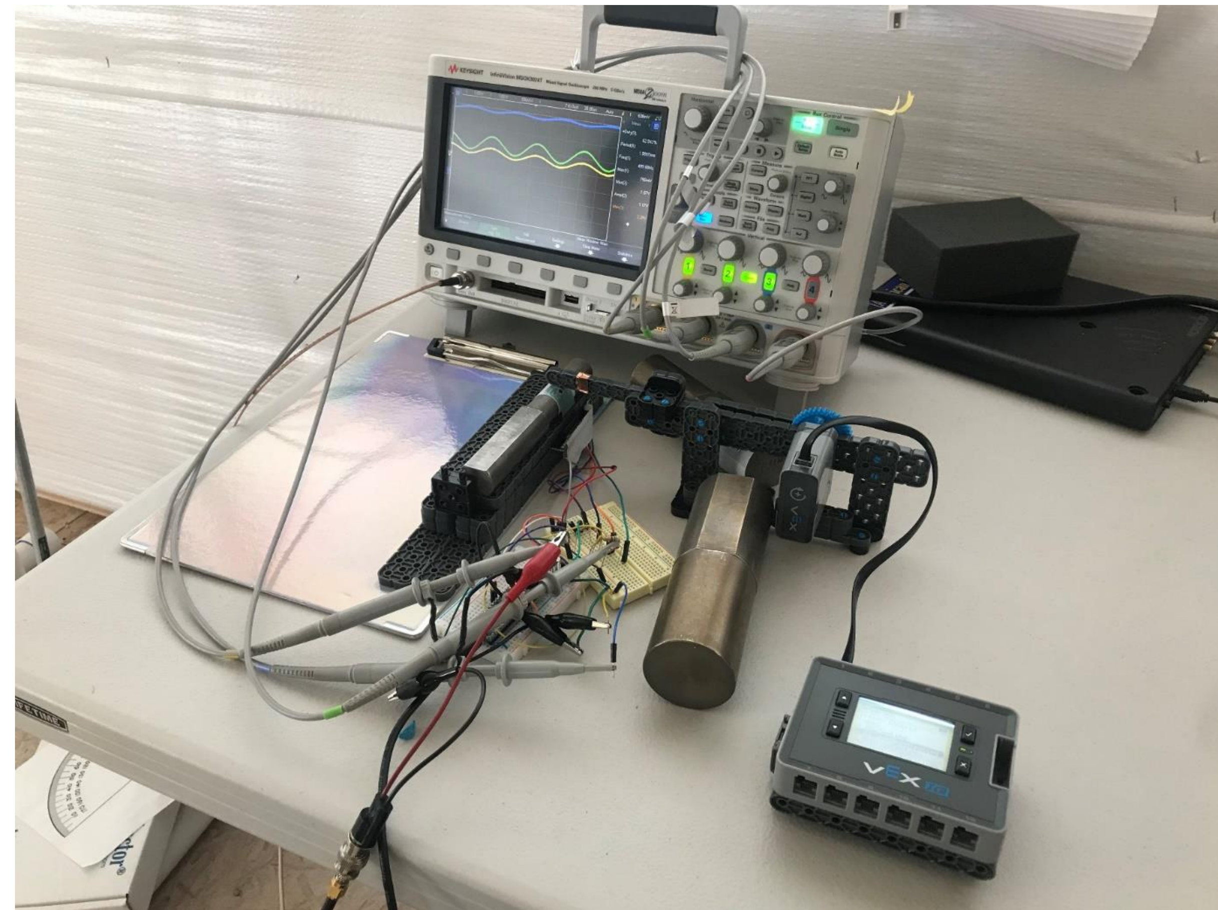
Dynamic RoC – ASI TEST003

ASI Procedure: TEST003

- Dynamic bend testing
  - 10mm ROC
  - 10k cycles in each bend direction (concave/convex) for 20k total cycles
- Establish Vdd and gain changes throughout the bending cycle
  - 15mm ROC



- Keysight Infinivision MSOX3024T Mixed Signal Oscilloscope
- Vex Robotics Kit
- 10mm Mandrel
- Teensy 3.4
- Custom Data Collection Software
- 3.3V LM317 Circuit
- OPA4002 configured as a non-inverting ~3dB amplifier

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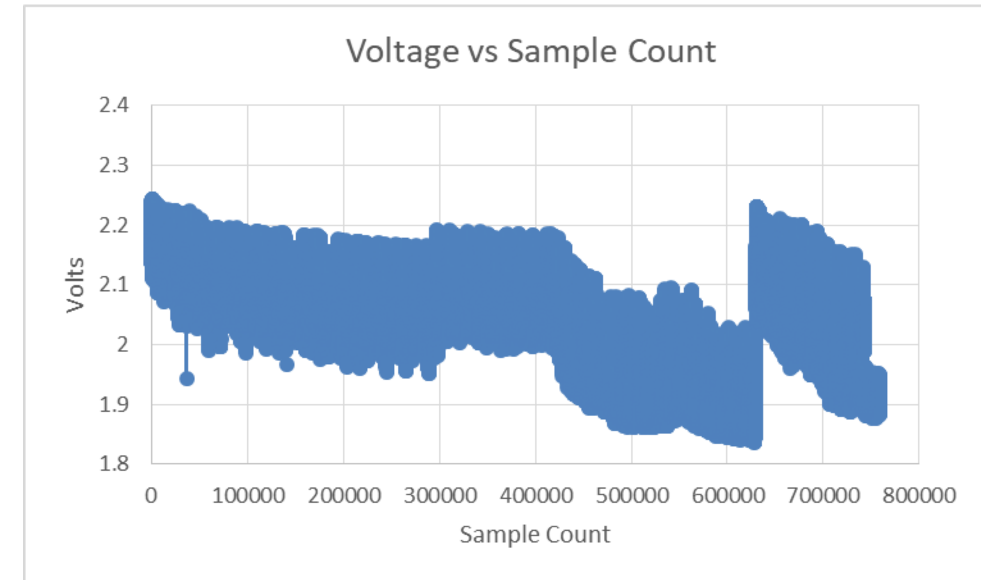
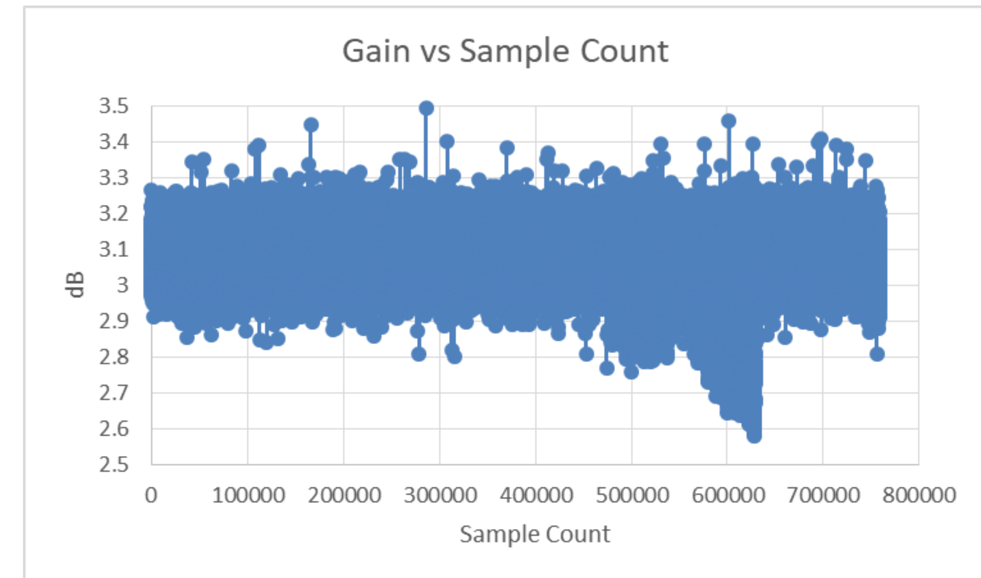
Dynamic Concave Bend Test 15-20k

- Vdd
  - Average: 2.04V
  - Minimum: 1.83V
  - Maximum: 2.24V
  - Std. Dev.: 88.1mV
- Gain
  - Average: 3.06dB
  - Minimum: 2.57dB
  - Maximum: 3.49dB
  - Std. Dev.: 0.0528dB
- Gain continued to hold relatively constant except for times of extreme Voltage drop





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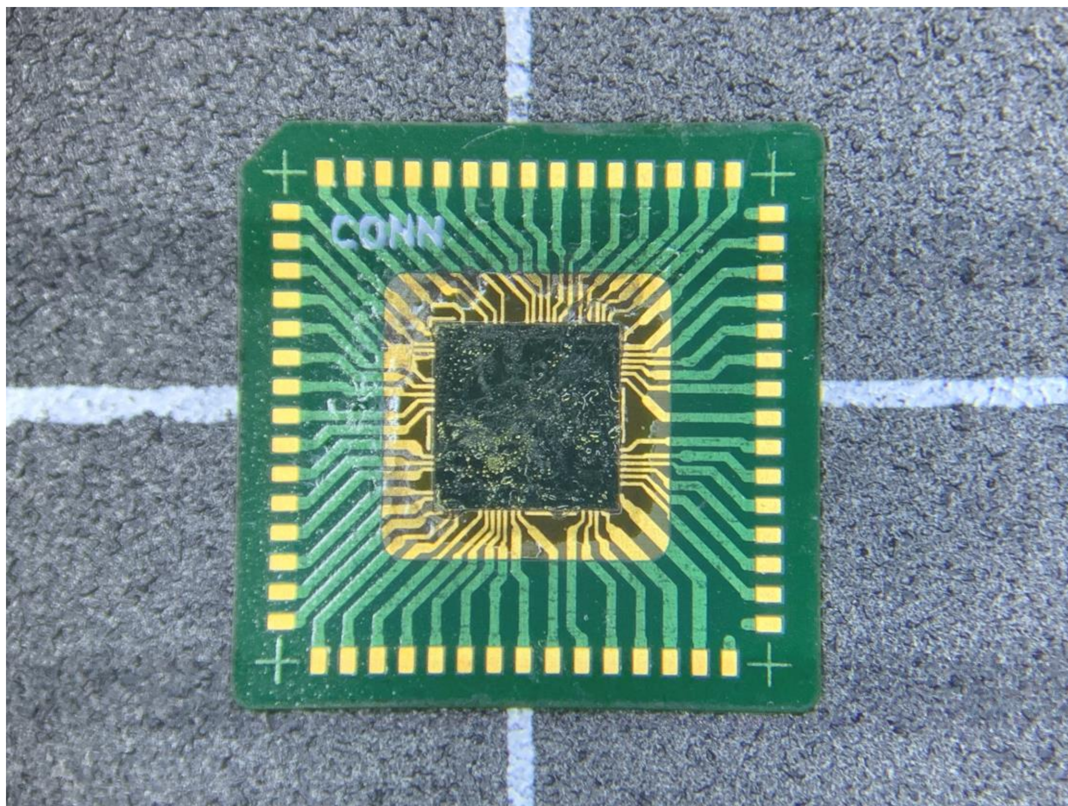
Temperature Reliability Test Setup

Equipment Used: Madell PnP, Hotronix Thermal Press, Multi-Meter, Yamato Drying Oven, CliniCool Freezer

BLE connectivity interposer with live AS_NRF51822P.fxd die

- Samples assembled PadDown with ACA + Cure
- 44 pin diode test on each sample (0.2-0.8V passing range)
- Elec. testing pre-, mid-points (each Temp Cycle), post on every pin/sample



Lowtemp Test

- 2 samples
- Troom pre-test
- -24C/72hr soak, test
- Troom/72hr test

HiTemp Test

- 8 samples
- Troom pre-test
- 75C/24hr soak, test
- 100C/24hr soak, test
- 125C/24hr soak, test
- Troom/72hr test
- 145C/24hr, test

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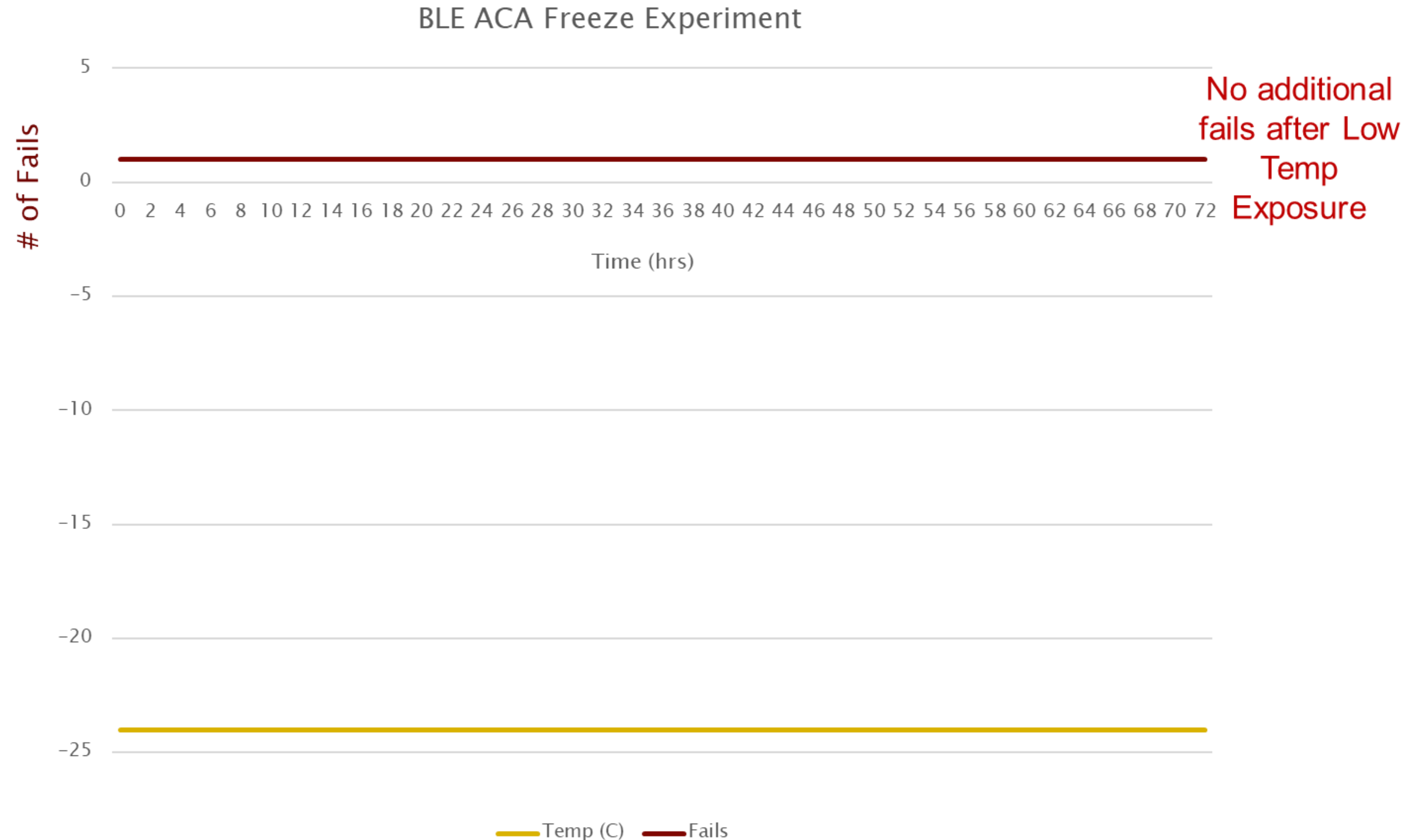
Extended (Low) Temp Soak Data

Single Open from Pre-Test is the only Pin Fail after -24C/72hr Soak

Low Temp Results

- -24C
- 1/88 pins failed initial pre-test
- No new fails after temp
- 100% post-temp yield



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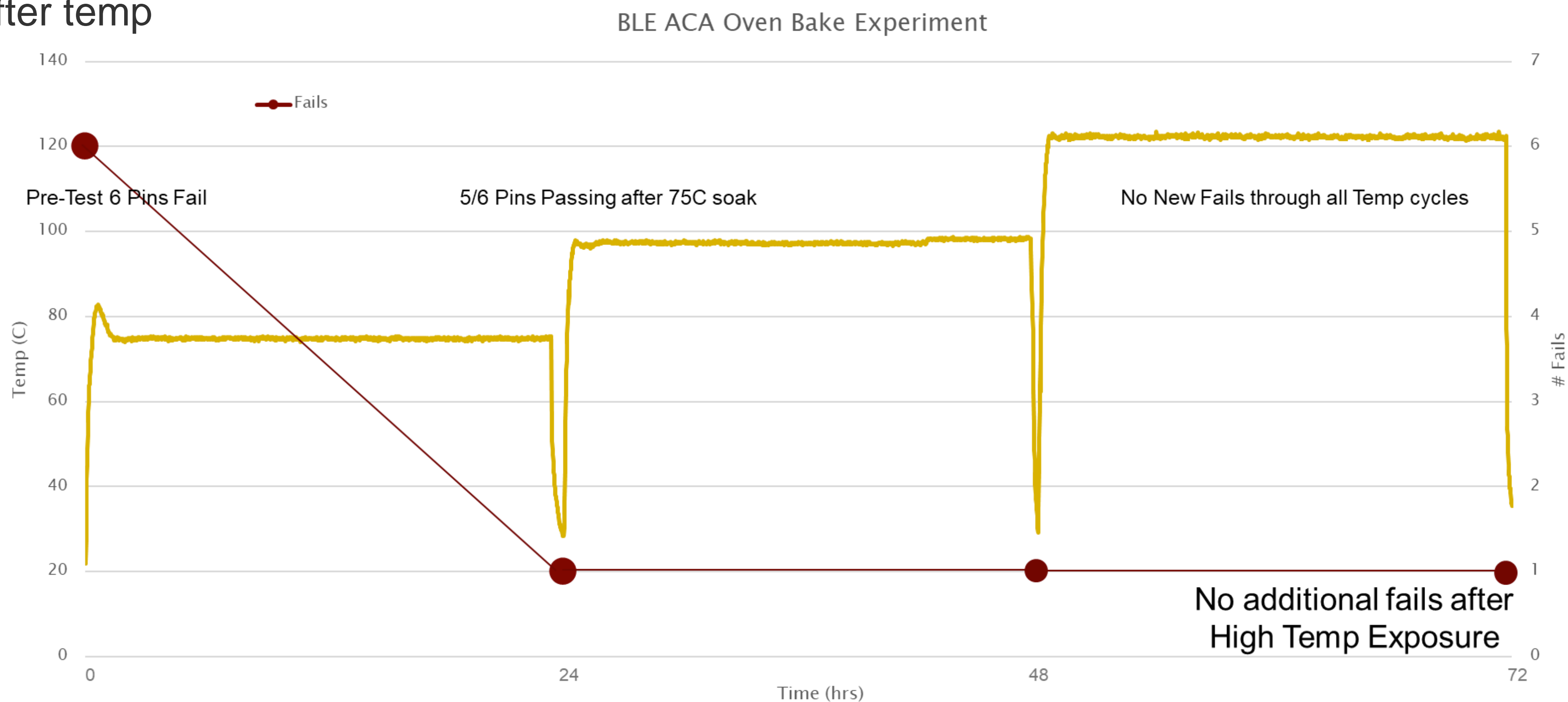
Extended (High) Temp Soak Data

Opens during Pre-Test 'repaired' after 75C Soak

High Temp Results

- 75C/100C/125C/145C
- 6/352 pins failed initial pre-test
- Only 1/352 pins failed after temp
- No new fails
- 100% post-bake yield



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Summary

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End-user Workshop hosted by Meta

- Microelectronics integration defines form factor limits for new VR/AR devices
- Electronic formats are not based on human requirements, but need to be
- Next generation VR/AR devices will integrate new electronics that include packaging specifically tailored to human requirements
- New VR/AR packaging requirements will drive some new electronic capabilities

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American Semiconductor - Boise, Idaho

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End-user Workshop hosted by Meta

American Semiconductor is the industry leader in ultra-thin advanced packaging. We develop state-of-the-art ultra-thin electronics technology.

- Founded Nov. 2001
- Over 21 SBIR wins
- 2-time Boeing SOTY

Member:

Packaging, Assembly, Test and Related Services

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Thank You

SoP packaging supported in part through Joint Development with HD MicroSystems

Thanks to Disco for their on-going support of ultra-thin processing requirements

Special thanks to Plasma-Therm for their support of special processing requirements

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