Advanced Protected Fan-In WLCSP

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Abstract

With the advent of bumped die new IC packages evolved: for low IO WLCSP (wafer level chip scale package), for high IO FC (flip chip) CBGA (ceramic ball grid array) and PBGA (plastic ball grid array). For low IO, protected CSP is an emerging and rapidly growing market. In 2020 the market exceeded $2B and is ramping to a forecast $2.5B by 2025.[1] Initially WLCSP, also known as FI (fan in), packages were built on the wafer with no active side protection evolving to single sided protection from a package built on the wafer[2] which transition to redistribution PSB (passivation stress buffer)[3], PSBs were used on FC wafers for high IO BGA packages. These provided acceptable performance initially, however as devices became more complex and reliability requirements increased, these processes no longer provided the required reliability. To attain higher IO capability and better reliability performance evolved to CSP[4] (non-WL) which allowed larger area for bump distribution and additional protection to the rest of the exposed die surfaces. Fully protected die CSP (without substrates or leadframes) was initially implemented with processes such as M-series utilizing a FO (fan out) process.[5] To obtain higher reliability 6-sided die protection afforded by M-series type processes require die reconstitution, expensive tapes, molding, and other operations generally required in a FO process which can feasibly be eliminated in a WLCSP protected FI process. American Semiconductor's Semiconductor-on-Polymer™ (SoP™) 300mm FleX-TM WLCSP is an advanced packaging process optimized for protected fan-in. FleX-TM produces the thinnest and lowest cost protected FI the industry today. Protected FI process innovations can improve performance in power devices, RF switches, die stacking and thin board applications. This article includes background on the evolution of CSP and the comparison of SOTA (state of the art) FI processes including FleX-TM.

Key words

Fan-In, Protected, Semiconductor-on-Polymer, WLCSP, CSP

I. Introduction

With the advent of bumped die new IC packages evolved: for low IO WLCSP (wafer level chip scale package) and for high IO FC (flip chip) CBGA (ceramic ball grid array) and PBGA (plastic ball grid array). The processes to support reliability requirements for bumped die packages evolved differently for high and low IO bumped die due.

Active side protection became important early on due to denser FAB technology for high IO die. This was driven by reliability issues related to bumping on traditional final passivation. The option selected to address these issues was a standard BEOL (back end of line) FAB processing to apply a PSB (passivation stress buffer). PSB had been developed earlier to protect molded die surfaces from the filler particles in the mold compound (filled epoxies) encapsulants in traditional plastic IC packages for WB (wire bond) devices. CBGA and PBGA packages also included encapsulants to protect the rest of the die and the bumps to improve reliability. These encapsulant materials included filled epoxies.

Low IO WLCSP, also known as FI (fan in), were built on wafers by adding bumps and redistributing the pads as needed. This resulted in the die being the package. However, without active side protection reliability issues ensued. This resulted in examining options to address the reliability issues observed. To maintain wafer processing active side protection options were explored. One option was to build the components of a plastic package on the active side on the wafer.[2] A simpler (and lower cost) option was to use PSB[3] as used on FC wafers for high IO BGA packages. The PSB

approach provided acceptable performance initially, however as devices became more complex and reliability requirements increased, these processes no longer provided the required reliability. To attain higher IO capability and better reliability performance evolved to non-WL CSP[4] which allowed larger area for bump distribution and additional protection to the rest of the exposed die surfaces.

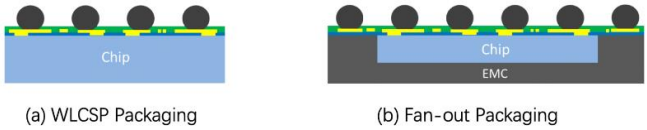

Figure 1 - WLCSP vs CSP FO. Source: Semiconductor Engineering Aug. 19, 2021

Various FO processes have been examined and noted in the literature which have additional die side protection. Small Small FO packaging processes are applied to die to create non-WL CSP.[5] Fully protected die CSP (surrounded on all 6 sides with similar material) was been implemented with processes such as M-series utilizing a FO (fan out) process.[6] To obtain higher reliability 6-sided die protection afforded by M-series type processes require die reconstitution, expensive tapes, molding operations required in a FO process. Resolving the reliability issues of unprotected die justified CSP for FI, but the added cost and process complexity is far from optimal.

An alternative approach that retains the simplicity of the wafer processing in PSB WLCSP would be to encase all sides of the die in PSB material replacing the encapsulate materials in the CSP options. This approach requires several changes to allow all side coverage of the device with PSB material which then acts as the encapsulate for the package. Emerging thin wafer processing facilitates the ability to provide protection to more than just the active side of the die. Earlier presentations and papers on SoP (Semiconductor-on-Polymer™) reported how this can be done for protecting the top and bottom of the die to improve mechanical reliability, as well as die performance, versus single sided or unprotected thin die. Comparison of 2-sided WLCSP, CSP and a 6-side protected WLCSP SoP process provides an understanding of cost and complexity of protected packaging technology.

II. Results and discussion

2-sided packaging has been the first step toward fully protected WLCSP capability. FleX-C Semiconductor-on-Polymer™ (SoP) is one example. This process, illustrated in Figure 2, has been shown to produce excellent mechanical reliability for thin silicon devices.[7] The process was developed to overcome the mechanical reliability and yield issues associated with thin die. The implementation of frontside and backside polyimide layers significantly reduced or eliminated die edge chipping and cracking that is common to thin die without protective coating. Robust ultra-thin ICs were first introduced to the Flexible Hybrid Electronics (FHE) market due to their ability to accommodate the stresses associated with deformation of flexible circuit boards (FCB). This capability was in addition to the primary FHE goal of maintaining the thinnest assemblies possible. Beyond FHE, the more generic application of this technology is being observed in chip-on-flex applications where previous use of surface mount packaging has resulted in unwanted product formats or reliability issues related to SMT assemblies failing during FCB deformation or bending.

SoP technology is being expanded to provide a WLCSP capability for 6-sided die protection. The new advanced packaging technology, referred to as SoP-TM™, provides full protection, but without the added complexity associated with FO processes used to produce CSP FI devices. FO processes such as M-series are utilized in FI production in order to provide the 6-sided protection needed for device reliability. FO processing provides 6-sided protection, but comes with a high price due to the necessity of including all the FO process steps and materials to manufacturer.

"Protected WLCSP" or P-WLCSP (WLCSP with 6-side encasement) processing provides the 6-side protection of non-WL or FO type processes, but without the cost and complexity. Protected WLCSP does not require pre-package die thinning, dicing or reconstitution and substantially reduces the equipment and process steps required for processing. Material costs are also reduced with the elimination of dicing tape and molding materials.

SoP-TM has been introduced as a high efficiency, low-cost, WLCSP process with 6-side protection. The 300mm process illustrated in Figure 4 utilizes polyimide for encasement. The process includes maskless processing and high temperature temporary bonding to enable the use of the widest possible selection of polyimides that can be balanced for stress and fully cured on all sides of the die. Final singulation can be accomplished with extremely fast laser dicing due to the fact that the protected WLCSP process produces polyimide filled scribe streets.

SoP-TM can be used to produce ultra-thin devices. The reduction of die thickness can be used to optimize and reduce through silicon via (TSV) size and pitch. The process capability that enables high-temperature backside polyimide curing enables feasibility for backside RDL (B-RDL) and heat sinks. CMOS silicon thicknesses for FEOL using standard bulk silicon is typically 10-15um, but can be adjusted thicker or thinner as needed to accommodate device

requirements. SoP processing can be used on both thick (bulk) and thin (SOI) silicon technology as it is independent of starting material type.

P-WLCSP may be most significant for RF devices that rely on SOI. The standard SoP-TM process results in some amount of handle silicon remaining. In this case, the buried oxide/handle silicon interface is unchanged with no change to device performance. High performance RF application can include full elimination of the handle silicon and eliminate substrate coupling capacitance. Low insertion loss backside PIs with Df < 0.003 @ 80 Ghz can be used. Handle Si trap regions can be retained if desired. Additionally, the backside encasement can be selectively removed in key areas to further eliminate parasitic issue. These high-performance features are applicable to improve performance.

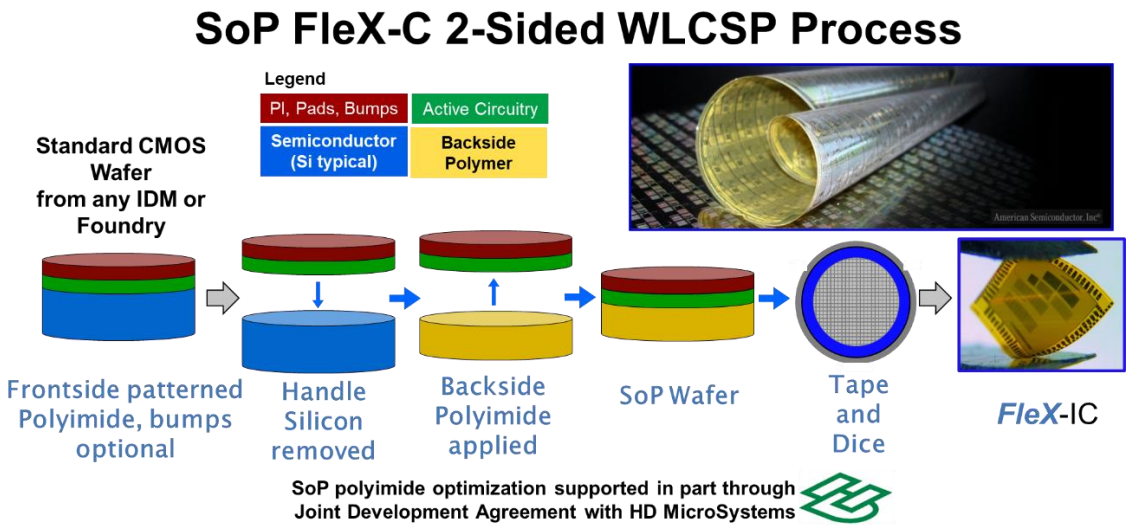

Figure 2 - Two side protected WLSCP Process

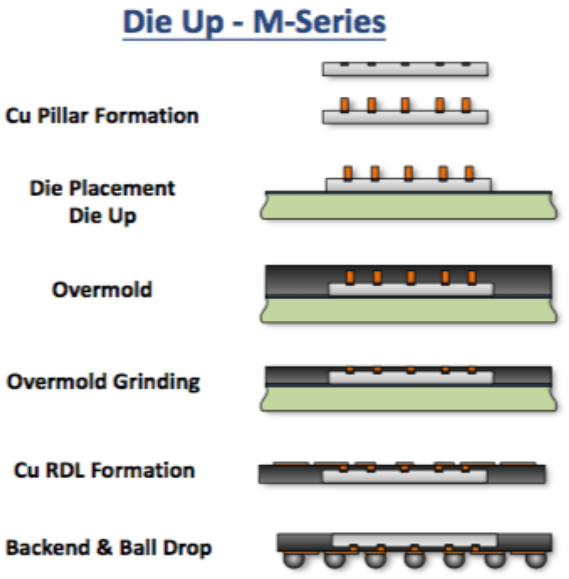

Figure 3 - M-Series CSP FO Process. Source: SemicondcutorEngineering Feb. 2018

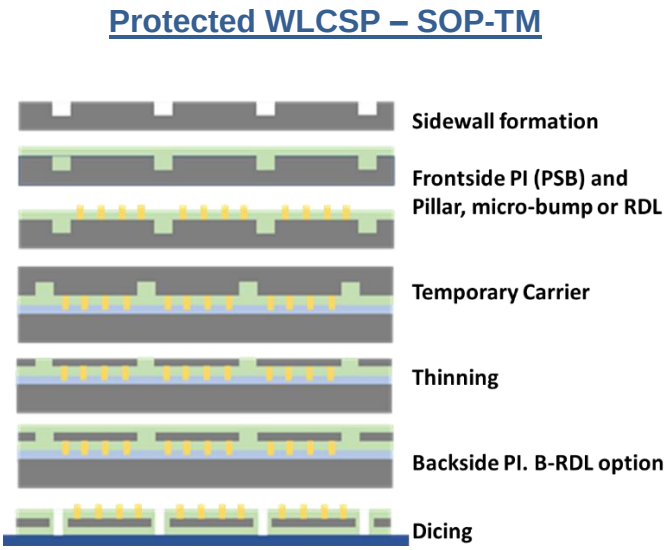

Figure 4 - SoP-TM Protected WLCSP

P-WLCSP processing is ideal for cost reduction and performance improvement in CSP FI applications. However, it's capability to produce robust ultra-thin devices can provide the needed building block for more complete SiP applications including those that rely on chiplets and heterogeneous integration. Higher pin-counts and thinner board assemblies are macrotrends in modern electronics. Reducing layer thicknesses, along with the opportunity to connect on top and bottom of die without any significant cost penalty is signficant.

III. Conclusion

An alternate approach to full die (all side) protection for CSP packages which retains the simplicity of WLCSP was presented. Full die protection has been widely adopted in a 6-sided FO approach to improve reliability, but with a high cost. The SoP-TM P-WLCPS process includes similar materials on all 6 sides which minimize uneven stresses on the die.

Continued WLCSP progress relies on further package reliability testing and data for relevant devices comparing standard WLCSP, 6-sided FO and 6-sided SoP. The necessary next step requires collaboration of device manufactures and the protected WLCSP packaging provider, as well as consideration of end user application requirements.

Whereas FO was the process that bridged the reliability gap for CSP FI, P-WLCSP may be the approach that will provide the die level building blocks needed for advanced multi-chip packaging solutions.

Acknowledgment

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