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Reliably Thin Electronics

SEMICONDUCTOR-ON-POLYMER (SoP™)
THE EVOLUTION OF THIN IC PACKAGING

October 2019

Doug Hackler
President & CEO

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Agenda

1. Package Thickness Scaling
2. Introduction to Semiconductor-on-Polymer (SoP) CSP
3. Ultra-thin applications
4. Heterogeneous Integration
5. Related reliability
6. SoP Technology Roadmap
7. Summary
8. Q & A

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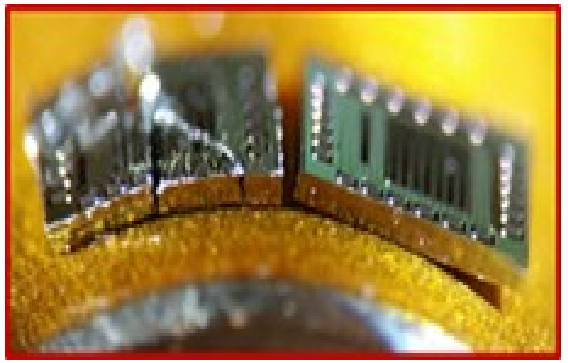
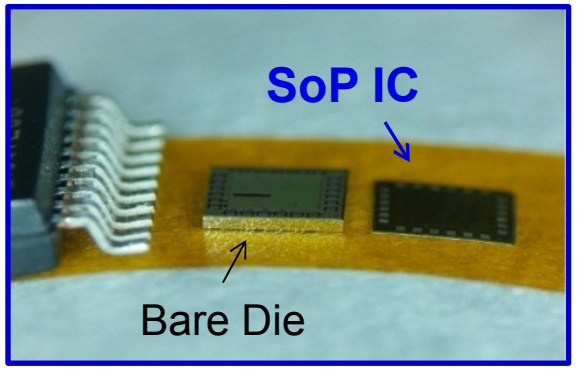
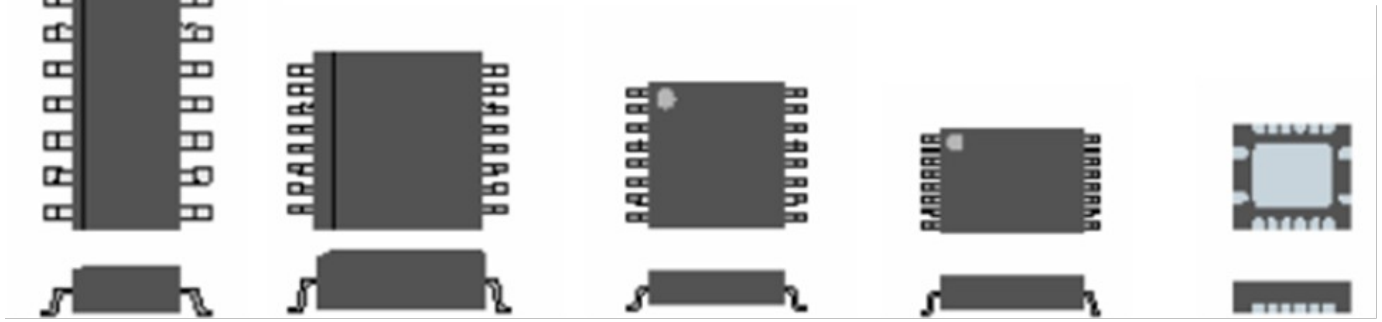
Package Thickness Scaling





- As systems become thinner, thin die and flexibility become important
- Thin systems bend and mechanically stress electronics
- SoP CSP was developed in response to the need for high reliability ultra-thin ICs
- SoP improves reliability for thin systems

Package Thickness Scaling



Attribute	SOIC-16 (D) [1]	SSOP-16 (DB) [1]	TSSOP-16 (PW) [1]	TVSOP-16 (DGV) [1]	QFN-16 (RGY) [1]		FleX-SoP (SoP) [3]
Length, mm	9.90 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	4.00 ±0.15	2.51	2.163±0.01
Width, mm	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15	2.51	2.283±0.01
Height, Max. mm	1.75	2.00	1.20	1.20	1.00	.075	0.025
Pitch, mm	1.27	0.65	0.65	0.40	0.50	RDL	<0.1
Footprint, mm²	59.40	48.36	32.00	23.04	14.00	6.3	4.94
Encapsulated	Yes	Yes	Yes	Yes	Yes	No	Yes (PI)
Weight, g	0.150	0.140	0.063	0.040	0.036	~.0008	.00023
SoP area save, %	91.6	89.8	84.6	78.6	64.7	NA	-

1. Quad Flatpack No-Lead Logic Packages, TI Application Report SCBA017D – February 2004 Morton, Wright
2. NHS3100, Bumped Die, NXP Product Data Sheet (NFC SOC)
3. AS_CY8C20 FleX-SoC Datasheet, American Semiconductor, 2018

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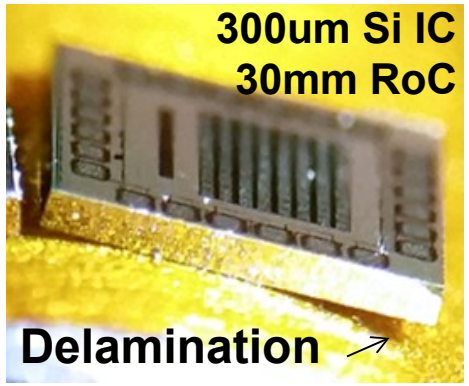
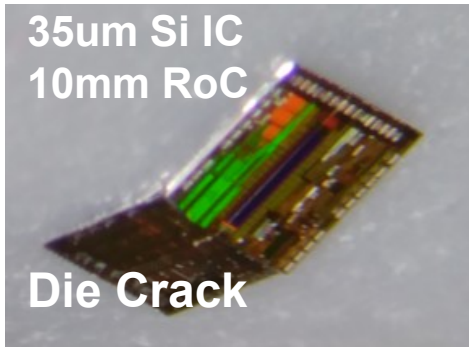
Thin Device Reliability

Radius of Curvature (RoC) Testing– ICs on PET boards





Thinning Method	Total Thickness (um)	Die Size (mm)	RoC Fail (mm)	Failure mode
Conventional thinning	300	5.0 X 5.0	30	Delamination
		2.5 X 2.5	12	Delamination
	40	2.2 X 2.2	10	Delam & Cracking
	20	2.2 X 2.2	10	Delam & Cracking
SoP WLCSP	28um (Si<5um)	2.5 x 2.5	5	PASS

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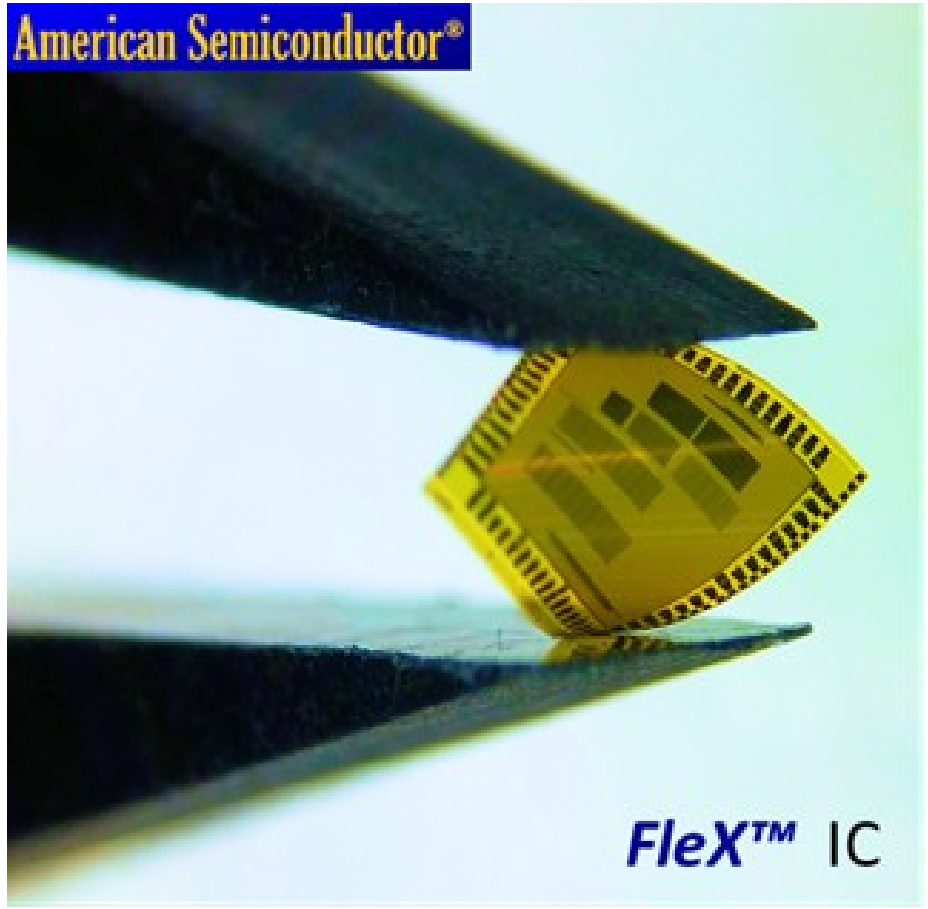
Introduction – SoP WLCSP



Semiconductor-on-Polymer
US Patent 9082881

- Semiconductor-on-Polymer (SoP) ultra-thin WLCSP process
- SoP CSP results IC material thickness less than possible with bare die
- SoP CSP improves thin device reliability
- SoP ICs (FleX-ICs) can be physically flexible

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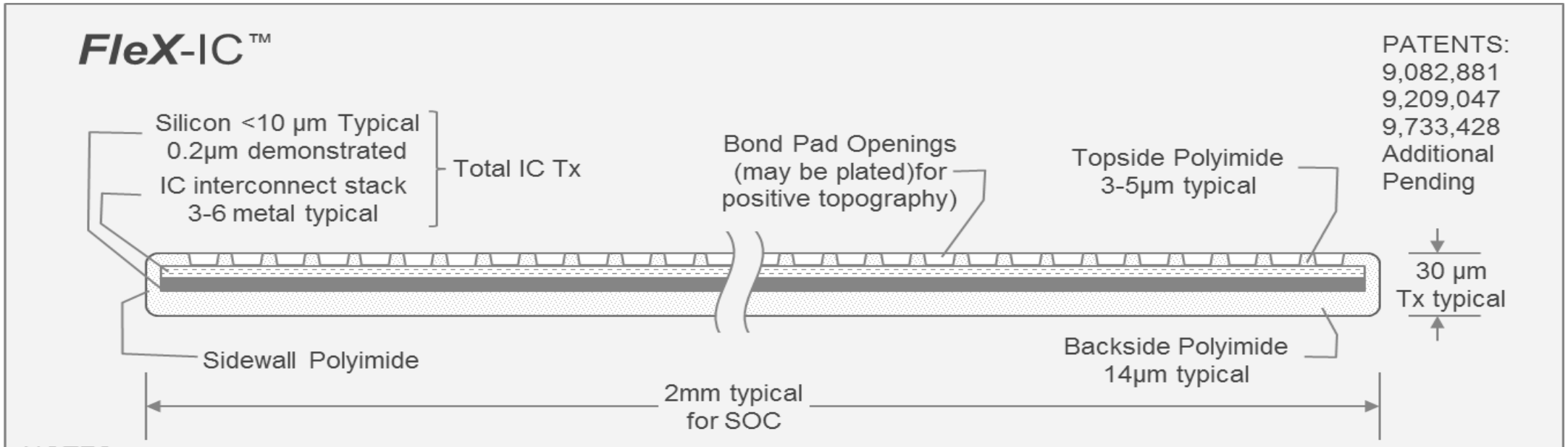
Semiconductor-on-Polymer



NOTES:

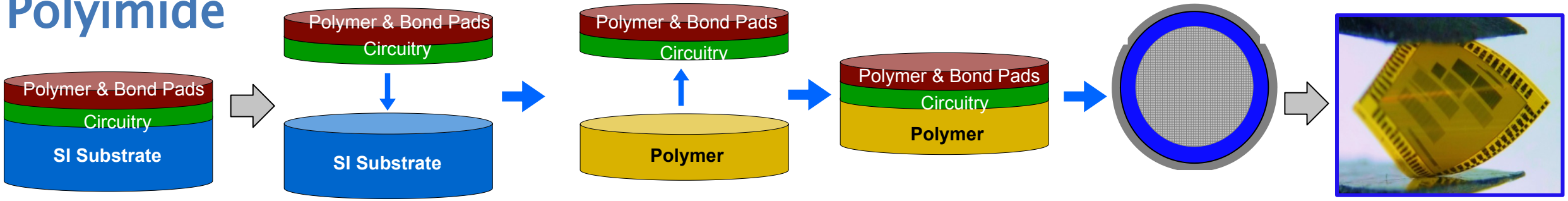
- Semiconductor-on-Polymer (SoP) is a wafer scale conversion process technology that results in fully coated ultra-thin wafers.
- SoP restores ultra-thin processed wafer mechanical stability for reliability during dicing, handling, pick & place and application.
- FleX ICs are the singulated devices from SoP processed semiconductor wafers.

FleX IC characteristics: Physical flexibility. Surface protection on all sides. Ultra-thin.
Alternative Descriptions: Advanced Package Technology (APT), Chip-scale-packaged IC (CSP), Embedded IC package, Ultra-thin Silicon, Wafer Level Package, Flexible IC, Ultra-thin IC, flexible chip

American Semiconductor Engineering Schematic PROPRIETARY Released	DESCRIPTION: **Semiconductor on Polymer FleX IC** **Physically flexible fully integrated chip-scale-package ultra-thin silicon. Wafer level processing with full polyimide coating.**	ORIGINATING ENGINEER: D. Hackler NOT TO SCALE

Basic SoP WLCSP Process

Frontside patterned Polyimide



Standard CMOS Wafer from any IDM or Foundry

Handle Silicon removed

Backside Polyimide applied

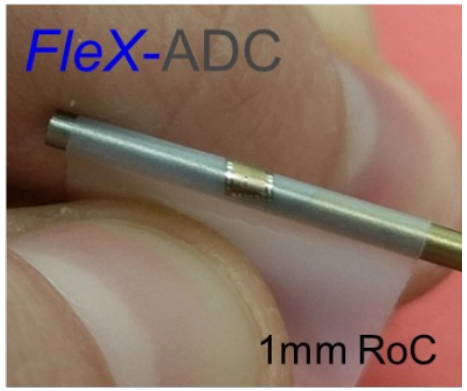
SoP Wafer

Tape and Dice

***FleX*-IC**

SoP polyimide optimization supported in part through Joint Development Agreement with HD MicroSystems

Thin Device Reliability



Test Results – non-mounted ICs

Thinning Method	Total Thickness (um)	Die Size (mm)	RoC Fail (mm)	Failure mode
Thin Die SOC	35 Si	2.16 X 2.28	10	Crack
SoP ADC	<5 Si	2.5 x 2.5	1	PASS (ASI)
SoP SOC	<15 Si	2.16 X 2.28	<5	PASS (Cypress)
SoP NFC	<15 Si	2.51 X 2.51	<5	PASS (NXP)
SoP RFID	<15 Si	1.66 X 2.05	<5	PASS (EM Micro)

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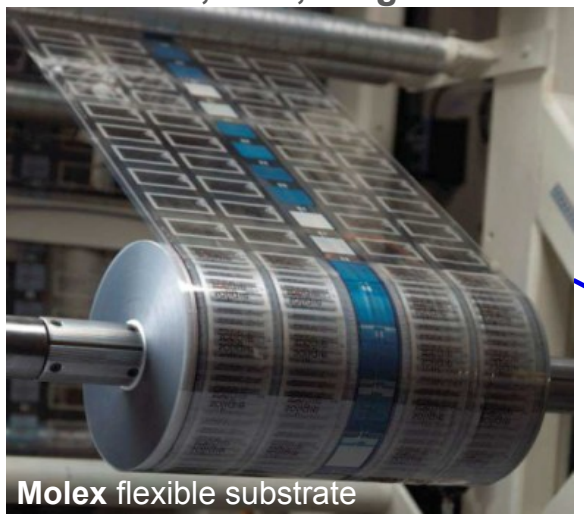
Flexible Hybrid Electronics (FHE)

Hybrid systems provide a flexible product solution that combines the best of silicon based components and flexible organic and printed electronics

Printed Electronics

Low Cost, R2R, Large Format



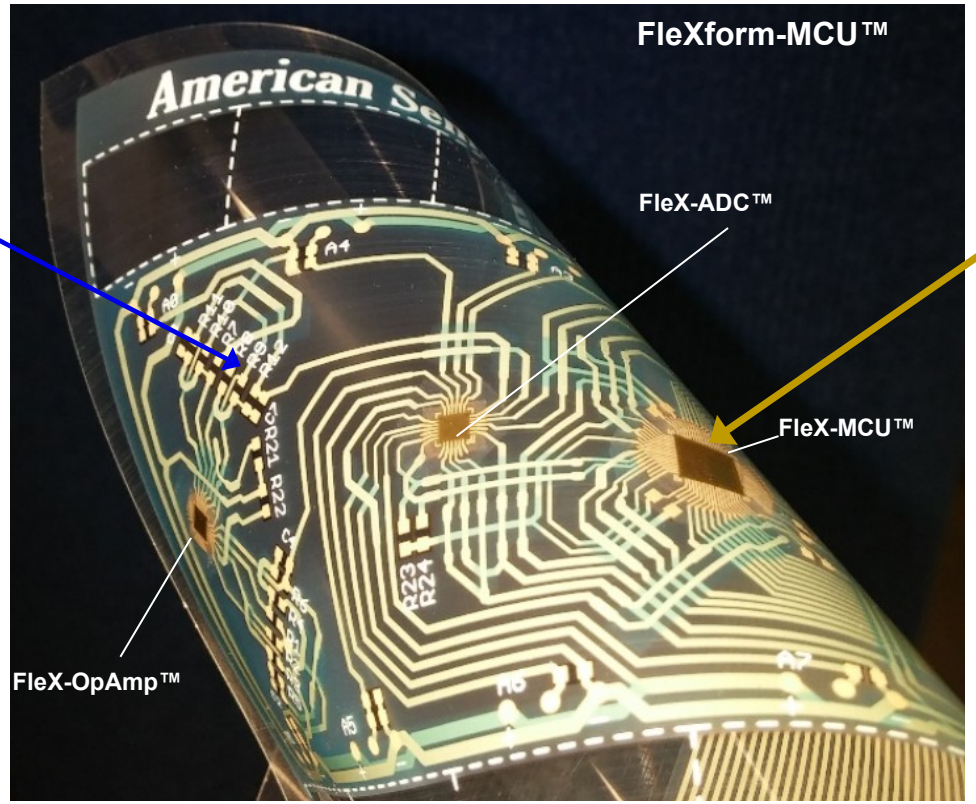
Printed Electronics

- Sensors
- Interconnects
- Substrates
- Displays

- Low Cost, Large Format
- Roll-To-Roll, Screen, Inkjet Print,

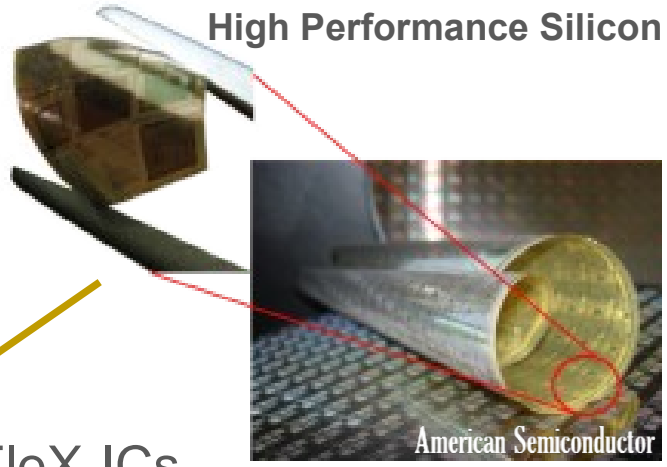
Flexible Hybrid System

Combination of printed materials and high performance components to create a new class – "flexible electronics."



Flexible *FleX*-ICs

High Performance Silicon



FleX-ICs

- Sensor Signal Processing
- Data Processing
- Data Storage
- Communications
- Low Cost, High Performance
- ***FleX*** is a Semiconductor-on-Polymer (SoP) conversion process that results in **chip scale packaging**.

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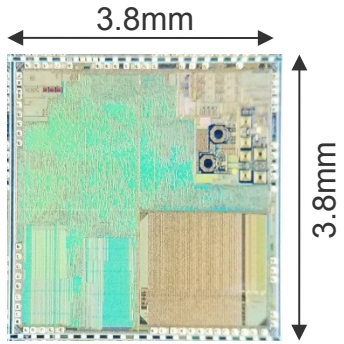
Ultra-thin Bluetooth®

AS_NRF51 SoP BLE IC

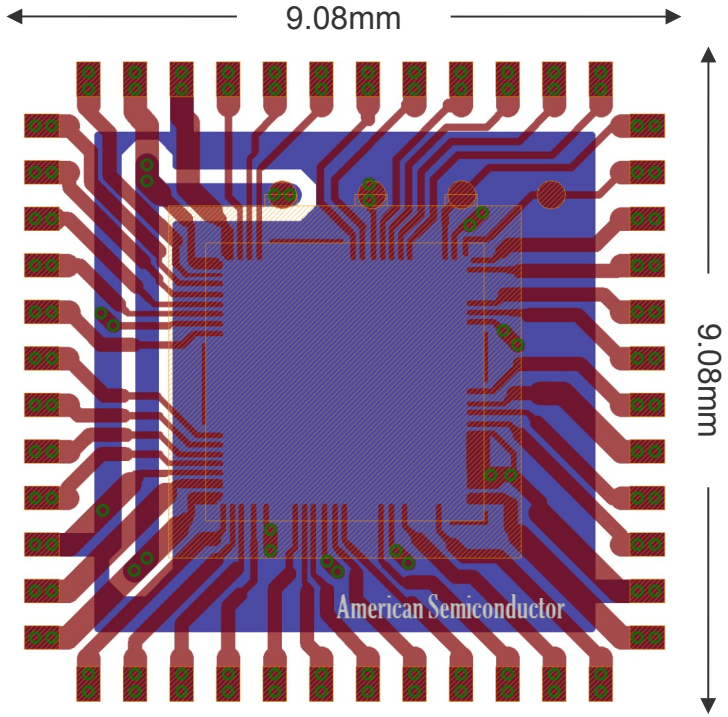
BLE: 2.4GHz Bluetooth Low Energy, 32-bit ARM Cortex-M0, 256kB Flash, 32kB SRAM, ADC, Temp Sensor
Package Thickness: 35um
Min. Pad Pitch: 100um



NORDIC SEMICONDUCTOR

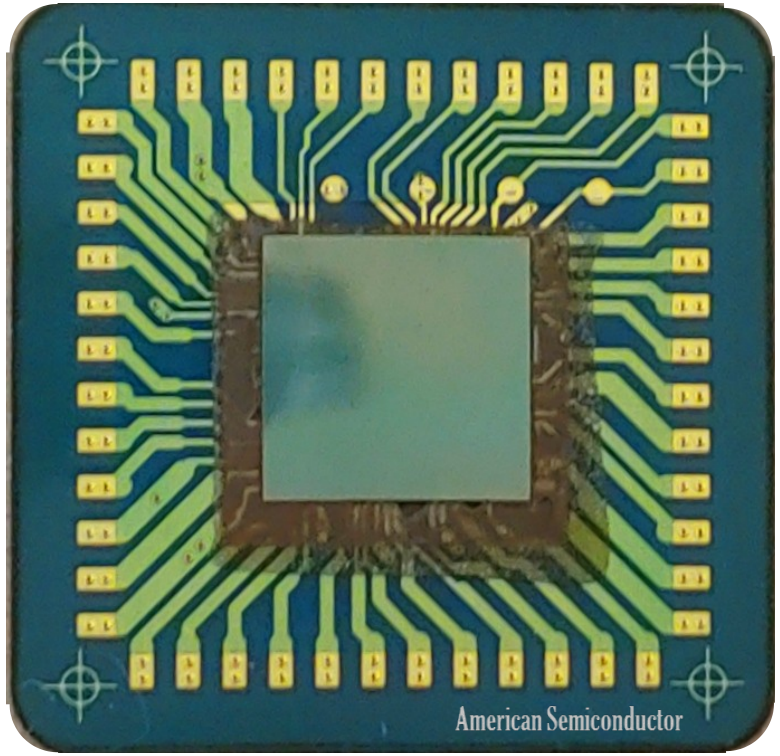
FleX-BLE Inlay

Die: 50um line/100um pitch
Periphery: 325um/650um pitch
Pyralux™ (~125um)



BLE FHE Assembly

Flipchip SoP DI (Direct Inteconnect)
SoP BLE (35um)
Flex Inlay (125um)
Total Tx = ~160um



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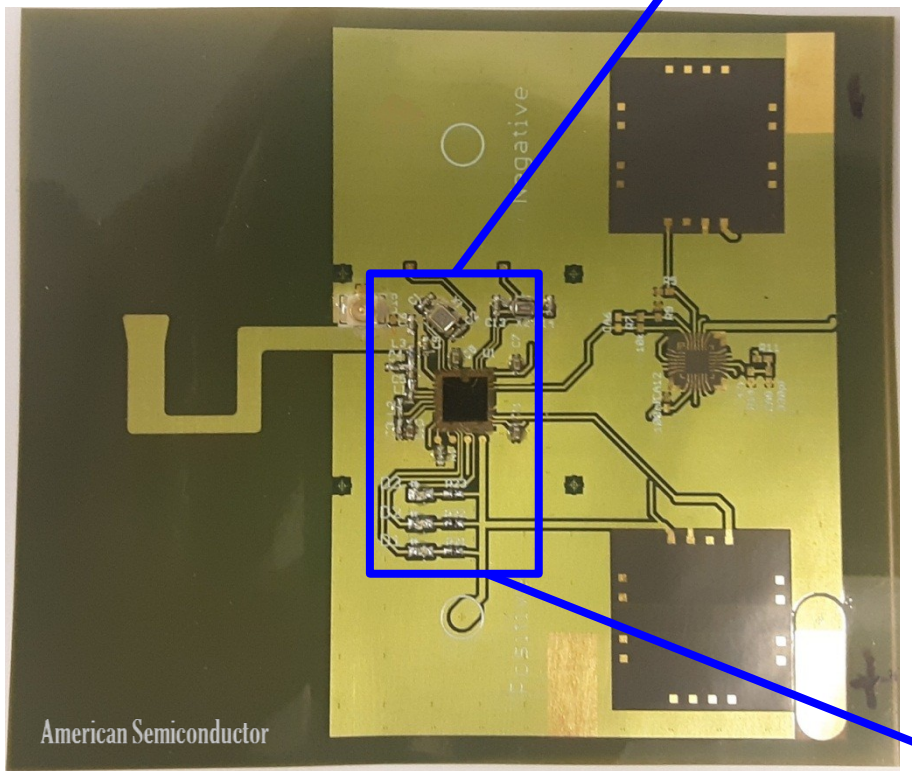
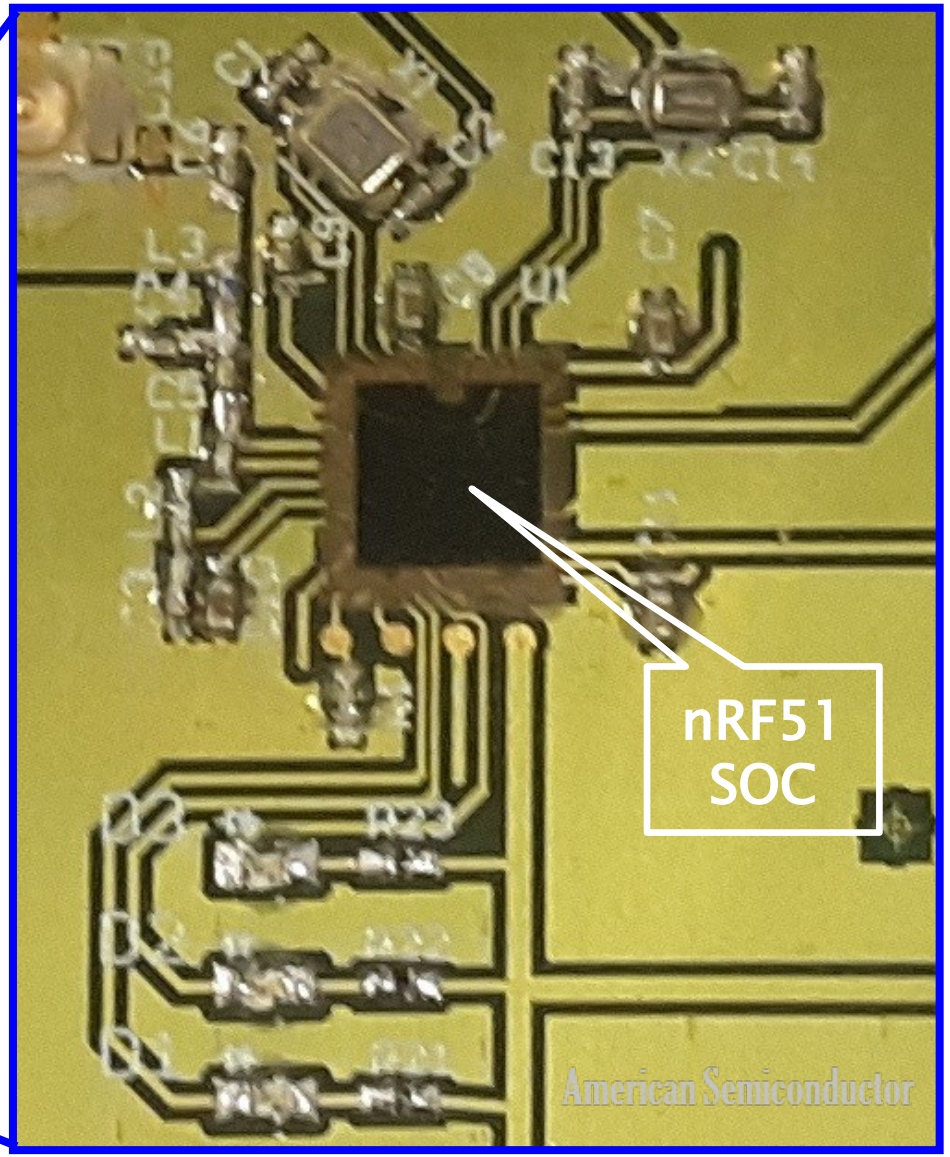
Preparing for Heterogeneous Integration

Bluetooth® Sensor Module

- Chips on flex
- Flip chip SoP SOC
- Quad OPAMP
- XO
- Caps
- Resistors





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FHE Test Procedures

Test	Conditions	ASI Procedure	References
High Temp Life	125°C	ASI TEST008	ISO 10373-1; JESD22-A108
Low Temp Life	-25°C	ASI TEST009	JESD22-A108
ESD	HBM and/or CDM	ASI TEST010	ANSI-ESDA-JEDEC_JS-001 & JS-002
Static Radius of Curvature	Concave/Convex Bend	ASI TEST003	ASTM D522-93a; ISO 10373-1; ISO 7816
Dynamic Radius of Curvature	Concave/Convex Bend	ASI TEST005	ASTM D522-93a; ISO 10373-1; ISO 7816
Axial Torsion	Twist Test	ASI TEST006	ISO 10373-1; ISO 7816
SEM Inspection	Post SoP Conversion	ASI TEST007	MIL-STD-883: M2018
Data Retention	150°C, non-bias	ASI TEST009	JESD22-A117; JESD-A103

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FHE Reliability Test Results

Test	Conditions	Results	Notes
High Temp Life	125°C	Pass	168 hours
Low Temp Life	-25°C	Pass	168 hours
ESD	HBM	Pass	4kV
Static Radius of Curvature	Concave/Convex Bend	Pass	1mm radius
Dynamic Radius of Curvature	Concave/Convex Bend	Pass	10,000 cycles at 5mm radius
Axial Torsion	Bend Test	Pass	90,000 cycles at 180° twist
SEM Inspection	Post SoP Conversion	Pass	4 metal CMOS delayering
Data Retention	150C, non-bias	Pass	500 hours

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FHE Reliability Tests in Development

Test	Conditions	References
Moisture Sensitivity Level	1) 1) 168hrs 85°C 85% RH 2) 2) 168hrs 85°C 60% RH 3) 3) 192hrs 30°C 60% RH	JESD22-A113
Thermal Cycling	TCB: -55°C to +125°C TCC: -65°C to +150°C	JESD22-A104
Highly Accelerated Stress Test	130°C 85%RH 33.3psi For 96 to 264hr	JESD22-A110E; MIL-STD-883 101C; JESD22-A102

- A key goal for engaging in this conference and community is to learn the critical issues and best approaches for testing and evaluating SoP
- We hope that you will provide your inputs and opinions

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SoP Technology Roadmap

SoP tech roadmap	Auto	Consumer Products	Logistics and Warehouse	IoT	Healthcare	STATUS	IC Market
Released Products Low I/O count, <50, 100um L/S typical	FleX-C (POR)	FleX-C (POR)	FleX-C (POR)	FleX-C (POR)	FleX-C (POR)	Released	A large portion of the IC market volume is low to mid I/O count typical of current and near-term SoP.
Lower Profile with Sidewall PI Enable ultra-thin, Reliable, I/O count <100, 80um L/S typical	FleX-C (POR) FleX-TM (R&D)	FleX-C (POR) FleX-TM (R&D)	FleX-C (POR) FleX-TM (R&D)	FleX-C (POR) FleX-TM (R&D)	FleX-C (POR) FleX-TM (R&D)	Near term R&D	
FUTURE SoP Advanced Packaging Highest performance, High I/O count, >100 with dense routing	FleX-ACSP (R&D)	FleX-ACSP (R&D)	FleX-ACSP (R&D)	FleX-ACSP (R&D)	FleX-ACSP (R&D)	Initial and Planned R&D	High I/O count market. Include heterogeneous integration, SoP in 3D and similar.

Summary and Next Steps

SoP CSP Summary

- SoP CSP provides an ultra-thin package type that utilizes polyimide encapsulation
- SoP CSP has been applied to a wide variety of CMOS ICs
- DCA and DI assembly will be used for thin systems
- Systems are becoming thinner
- Continued thickness scaling is a key roadmap issue
- Thickness scaling will extend to theoretical minimums

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Summary and Next Steps

SoP CSP Next Steps

- SoP WLCSP capacity coming on-line
- Ultra-thin IC packaging demonstrations and reliability data
- Reliability leaders are encouraged to test and model new characteristics of mechanically stressed ultra-thin electronics
- Sharing and presenting ultra-thin package and integration data will facilitate faster scaling

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Thank You

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