Ultra-thin Flip-Chip Assembly for Heterogenous and Hybrid Integration

Douglas Hackler1, and Edward Prack2  
1American Semiconductor, 2MASIP, LLC  
6987 W. Targee St  
Boise, Idaho83709 USA  
Ph: 208-336-2773; Fax: 208-336-2752  
Email: [doughackler@americansemi.com](mailto:doughackler@americansemi.com)

Abstract

Flip-chip packaging of thin-die, in fact any packaging of thin-die, is one of today’s most significant challenges for die handling. Despite the difficulties presented as the thickness of chips continues to decrease, the wide range of applications they have enabled across multiple industries has led to increasing interest, as evidenced by the growth in the cumulative total number of publications on thin silicon based electronics, including Ultra-Thin Chips (UTCs), thinning of Silicon-on-Insulator, and wafer thinning. Smart devices including labels, loggers, wearables, implantable medical, and IoT are in demand. A key area of difficulty in the packaging of thin chips comes from removing the individual chips from dicing tape due to the adhesive nature of the tape and die cracking and edge chipping characteristic of thin die.

As the industry continues to embrace the benefits afforded by thin devices, two trends are being witnessed. Devices continue to grow larger in area and thinner in thickness. American Semiconductor’s automated production process for packaging and assembly of chips ≤35um in thickness will be presented. This includes details regarding needleless die eject, pick tip design for ultra-thin devices, ultra-thin flip-chip interconnects, thin-chip overcoat, process controls, and assembly on flexible circuit boards (FCB).

Key words

Chip-scale-package, Fan-In, Fan-Out, Antenna-In-Package, Semiconductor-on-Polymer, Direct Chip Attach

# **I. Introduction**

As the industry continues to embrace the benefits afforded by thin devices, two trends are being witnessed. Devices continue to grow larger in area and thinner in thickness. Flip-chip packaging of thin-die, in fact any packaging of thin-die, is one of today’s most significant challenges for die handling. Despite the difficulties presented as the thickness of chips continues to decrease, the wide range of applications they have enabled across multiple industries has led to increasing interest, as evidenced by the growth in the cumulative total number of publications on thin silicon based electronics, including Ultra-Thin Chips (UTCs), thinning of Silicon-on-Insulator, and wafer thinning. Smart devices including labels, loggers, wearables, implantable medical, and IoT are in demand. [1]

Semiconductor-on-Polymer™ (SoP) is a Fan-In (FI) CSP technology that has been developed to provide robust ultra-low volumetric chips. The process was initially developed in response to the need for ultra-thin flexible devices required for flexible-hybrid-electronics (FHE). Ag-on-PET flexible circuit board (FCB) assembly is very similar to chip-on-flex and is evolving to include multi-chip capability using ultra-thin chips as shown in Figure 1. FHE, Chip-on-Flex, and advanced IC packaging are often developing under different technology roadmaps, but all include the need for thinner device capabilities.

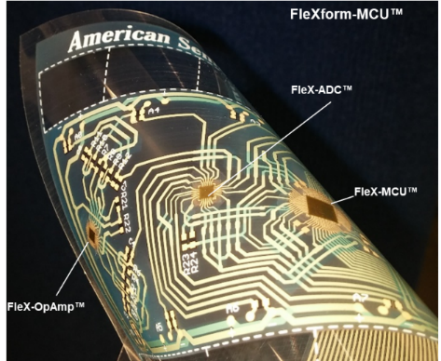


Figure –1 FHE Ag-on-PET FCB with multiple SoP FC

SoP offers an integration path for ultra-thin die into conventional IC packaging. This allows thinner and more reliable IC packaging for Fan-In (FI) and for Flip-Chip (FC) packaging. In addition, SoP provides unique paths to integration into traditional Package-on-Package (PoP) and Fan-Out (FO) packaging as well as integrated functionality such as Antenna-In-Package (AIP).

**II. Ultrathin FI CSP**

Ultra-thin device packaging begins with the fabrication of the smallest possible volume IC, i.e. Chip Scale Package (CSP) devices that are similar to the size of bare die. American Semiconductor’s wafer level FI CSP production process for packaging chips with ≤35um total package thickness is a typical example of SoP capability, Figure 2. The device shown is implemented with polyimide that is essentially clear. Polymer selection can include opaque materials if beneficial to the targeted application.

In SoP the backside polymer coating provides the mechanical structure that enables the semiconductor materials stack to be thinner than what is feasible for bare die. The polymer coating of the frontside and backside provide the dielectric necessary for improve reliability and enable routing for FI connections. SoP chips are exceptionally thin and relatively two-dimensional in nature. The thin CSP design was initiated in support of general advanced packaging challenges such as chip stacking where the thin device reduces chip step heights.

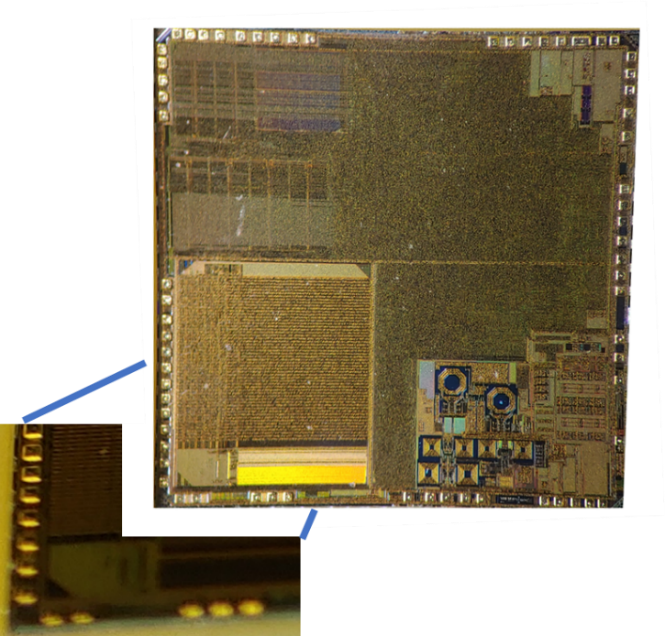
****

Figure2 – AIP SoP CSP IC. CSP IC + bumps have a total thickness of less than 45um

Die protection has been a challenge for CSP/FI die particularly for thinner die. The SoP process provides die protection in 2 sides (top and bottom) or 6 sides (top, bottom and sides). The novel 2-sided CSP polymer coating enabled extreme thinning of CMOS devices. It is now common to thin bulk silicon ICs in SoP to as little as 2um of silicon and retain the ability to handle and process them as individual chips with little concern for die cracking and edge chipping. In addition to being extremely thin, the devices with silicon thicknesses less than 15um have proven to have a high degree of physical flexibility that has been proposed as a reliability improvement for systems that utilize thin-PCBs subject to physical deformation. This protection has been demonstrated in the improved die strength noted in earlier publications.[2] The next-generation of the SoP WLCSP process includes 6-side polymer protection.

Various approaches have been used to improve reliability for CSP/FI packages. They include 2-sided die with tape backside protection [3] and 4-sided molded sidewall protection was proposed but was implemented as 5 [4] or 6 sided [5] epoxy protection. The 6-sided epoxy protection has been implemented to improve reliability of a FI phone component.[6] The SoP polymer protection is a simpler wafer level process flow and most likely a more cost-effective approach to die protection then backside films and molded side protection that have been noted above.

**III. SoP in ultra-thin FC packaging and FO**

SoP chips have been used in FC packaging for thin-systems using flex substrates. SoP chips can also be used in a variety of FC manufacturing processes. One example is the BLE® flexible-hybrid-electronic (FHE) device, Figure 3a-c. Nordic’s Bluetooth® SOC shown in Figure 3a is the basis for this assembly. The pads shown on the topside of the assembly in Figure 3b are connected in FHE copper on polyimide conductors in a face up configuration with flip-chip ACF/ACP flex configuration. The flex substrate could be exposed on the backside where they could be bumped to produce a thin conventional FC-BGA package as shown in Figure 3c. In this case, a flip-chip integration of a SoP chip has been applied to a Pyralux® flex interposer for use in wearable and flexible applications. In this implementation DCA includes needleless die eject, pick-tip design optimization for ultra-thin devices and ultra-thin flip-chip interconnects using anisotropic conductive adhesives for assembly of micro-bumps as small as 50um. If required thin-device overcoats or laminates that maintain system thinness can be tailored to specific reliability requirements.

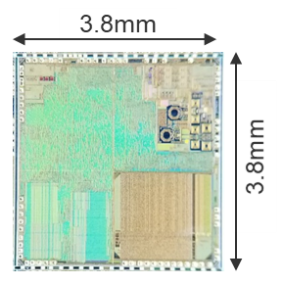


Figure 3a - NRF51 BLE IC

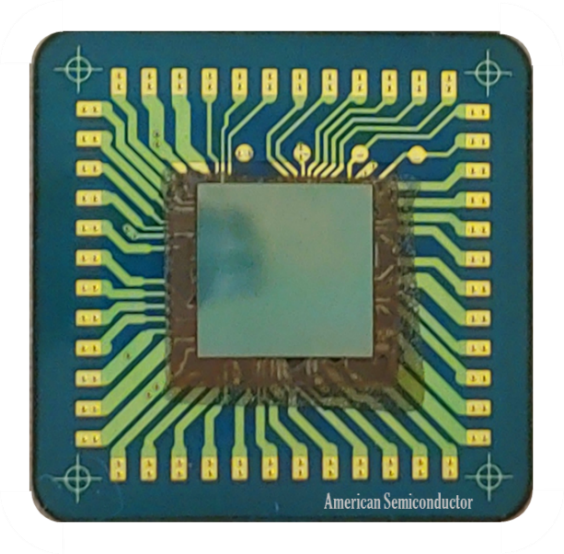


Figure 3b – BLE FO Package (Current frontside image with FC SoP NRF51 SOC)

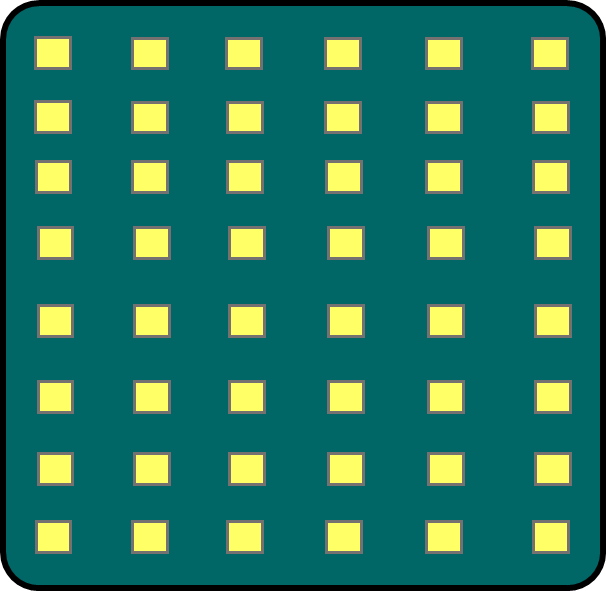


Figure 3c – Backside illustration of BLE FO Package configured for BGA

This approach can be expanded to include a variety of FO manufacturing approaches where the SoP based thin chip(s) with single or double sided IO can be incorporated into a Package-on-Package (PoP)assembly flow or as a stacking layer in FO stacks.[7] In addition this approach can be extended to multi-chip system in package (SiP).

A key area of difficulty in the packaging of thin chips is the impact on yield from removal of the individual chips from dicing tape. This is most significant in multi-chip assemblies were failure of any one chip will results in system failure. Die cracking and edge chipping are common problems inherent in thin-die. The use of SoP significantly improves die strength and when coupled with needleless chip pick can provide improved manufacturability for SiP and HI.

**IV. SoP FC and AIP**

SoP FC with antenna integration has been demonstrated for NFC and Bluetooth® systems. One of the earliest demonstrations is the implementation of AIP for ultra-thin data logger applications, Figure 4. In this case a SoP SOC (system-on-chip) is DCA assembled on substrate with the 13.56 MHz antenna (used for NFC-near field communication applications) with pads for external antenna, power and ground connections.

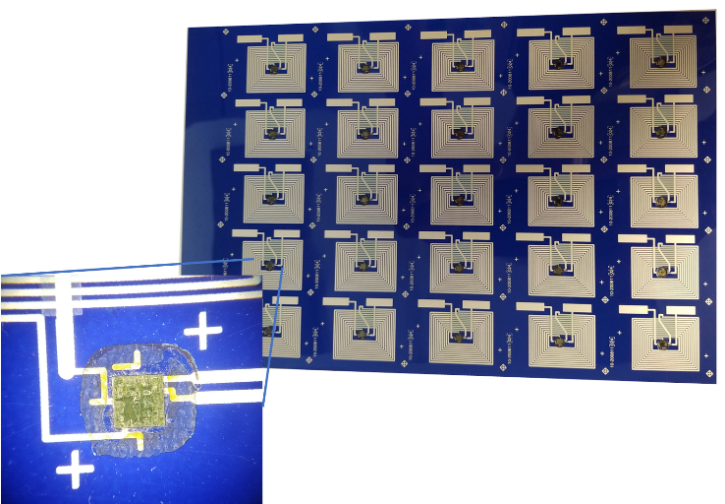


Figure 4 – AIP panel prior to encapsulation

In this application, the thin AIP device is laminated between a graphic protective layer and a thin flexible battery to support data loggers that can be applied to individual items such as vaccine vials shown in Figure 5. This package innovation results in the ability to apply SOC capability including ARM core, flash memory, temperature sensor, antenna and a thin flexible battery in a device that can be applied like a label to provide user cell-phone temperature verification of efficacy related to temperature sensitive pharmaceuticals and anti-counterfeit authentication. In additionally, these can also be used without batteries for applications such as embedded anti-counterfeit, business cards and wearable temperature sensors.



Figure 5 – Left: Thin data logger inclusive of SoP AIP, Right: Data logger applied to 10 ml vaccine vial.

The flex Bluetooth® AIP with a 2.4 GHz antenna, SMTs, SoP Bluetooth chip and interconnects is another example as shown in Figure 6a and 6b.

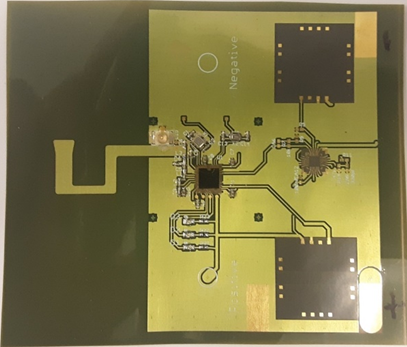


Figure 6a – BLE SOC, SMTs, Antenna and sensor connections

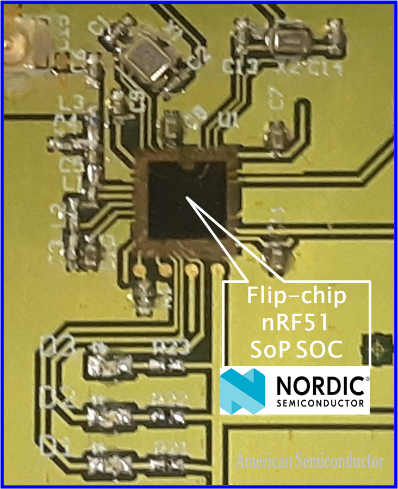


Figure 6b – Detailed view of Bluetooth package FC and SMT

These integrated thin die and antenna assemblies on flex can incorporate connections for power and IO from pads on either side of the flex for interconnect to other assemblies including other types of IC packages or modules. For example, wireless connectivity could be achieved by attaching to the backside of a current 2-sided FO package or other assemblies.

# **V.** **Conclusion**

Ultra-thin die are desirable for attaining thinner packages and provide routes for more space efficient electronic IC packages, assemblies and modules. Ultra-thin die reliability has been a challenge in production and assembly. Ultra-thin SoP packaged die are now available and provide a path to address production and assembly reliability challenges.

In this paper we have shown how SoP CSP which was initially targeted to flexible hybrid electronics can be applied to IC packaging. These applications include advanced packaging approaches such as FI, FC, and FO. In addition, FHE and SoP concepts can be applied to AIP IC packaging and multi component systems such as SiP, heterogeneous integration and PoP (Package on Package).  It can be further developed to enhance die-to-die stacking. This paper provides a glimpse of the potential of harnessing technology from multiple technology silos to accelerate high performance/low cost IC packaging. [8] In this case FHE (which includes RtR and additive manufacturing) and IC packaging. Further work will be required to flesh out cost effective production and commercial application of the examples noted as well as developing new possibilities.

**Acknowledgment**

We would like to acknowledge the work of the ASI team to produce and evaluate the SoP parts and assemblies that demonstrate the potential noted in this paper. Additionally, we acknowledge the support and advanced packaging materials provided by HD MicroSystems.

**References**

1. Parrish & Gillespie. (2019), Thin is In: The Challenge and Solution of Picking Thinner Die. Royce Instruments. Jun 20, 2019, [www.vtekusa.com](http://www.vtekusa.com)
2. D. E. Leber, et al, “Advances in Flexible Hybrid Electronics Reliability”,*2017 IEEE Workshop on Microelectronics and Electron Devices (WMED)*, May 2017.
3. Adwill backside coating tape <https://www.adwill-global.com/en/tape/coating.html>
4. T.Strothmann, S.Wook Yoon, Y.Lin “Encapsulated Wafer Level Package Technology (eWLCSP)” 2014 ECTC pp931-934
5. B.Rogers, C.Scanlon, T.Olson “Implementation of fully molded Fan-out packaging technology” 2013 IWLPC, San Jose, CA, pp S10-P1-1 – S10-P1-6
6. DECA M-Series https://thinkdeca.com/deca-technologies-transforming-electronic-interconnect/m-series/
7. N.Chhabra “Freescales Redistributed Chip Packaging (RCP) Ready for Production” June, 2010
8. E.Prack “IC packaging directions and challenges” invited keynote for ICPST-32, Chiba, Japan, 6/24-26/15